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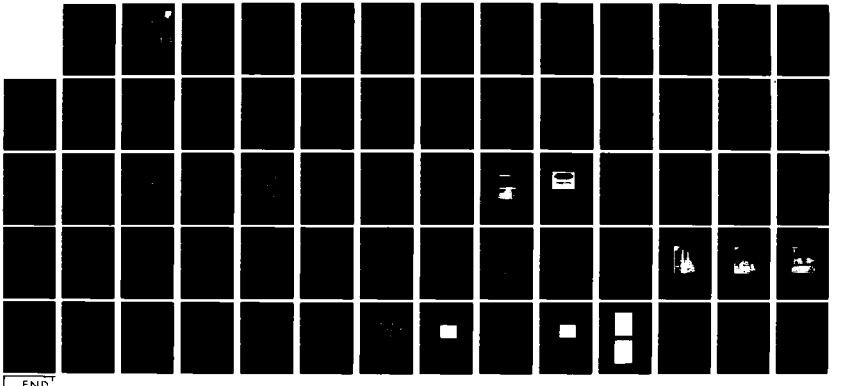

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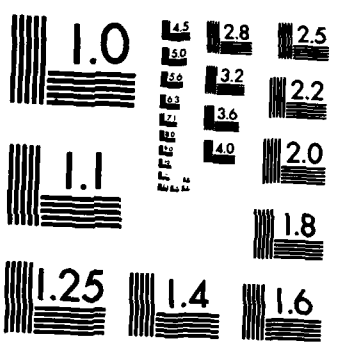

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RADC-TR-82-321
Final Technical Report
December 1982

HIGH SPEED CCD DESIGN

Rockwell International Corporation

J. A. Higgins

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

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The use of GaAs in a CCD structure should provide good transfer efficiencies at clock frequencies in excess of 1 GHz. These high clock speeds imply that high speed analog signal processing algorithm can be implemented which can be useful in the front ends of high speed communication systems. This effort has been designed to investigate the fabrication of planar CCDs using ion implant technology and to design and fabricate support circuitry and rf hardware necessary to drive 4 phase CCDs at clock frequen-

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cies higher than 1GHz.

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1.0 INTRODUCTION

The subject of this report is a one-year, one-man level program that was intended to be a source of support for the general goal of developing the high speed GaAs CCD device. It was also intended that this program would last three years and possibly grow in manpower. However, the program was cut short at the end of one year but not before progress was made and experience gained that was useful to the further development of the GaAs Charge Coupling Device.

The two principal activities of this program were concerned with the most pressing questions concerning these devices. The first question was whether the active layer design necessary for high speed charge coupling device action could be fabricated using a GaAs process which was suitable to the fabrication of GaAs FET Integrated Circuits, i.e., whether the CCD device could be made by ion implantation. This question was prompted by the need to develop and provide support circuitry for the GaAs CCD.

The GaAs CCD is expected to provide high charge transfer efficiencies at clock frequencies in excess of 1 GHz. To provide the proper clock waveforms at these frequencies is not a simple task especially if there is to be interchip connection of these gigahertz signals. The problems of ringing and phase control of such clock signals becomes very difficult even with the most carefully designed and well executed hybrid technology. Therefore, it is considered necessary to combine the CCD and the support circuitry monolithically on one GaAs chip and this task became the second principal activity of this program.

The problems addressed by this program concerned fabrication of the CCD by ion implantation and the design and fabrication of support circuitry necessary on a first cut basis.

In this report, the technical approach to the two tasks presented are separately detailed in the second and third chapters with summary and conclusions supplied in the final chapter.

2.0 GaAs TECHNOLOGY

2.1 Active Layers for GaAs CCDs

From a materials point of view, the GaAs CCD is a single n layer grown on a substrate. The substrate is semi-insulating if the CCD is to be a high speed CCD. Electrodes are placed upon the top surface of the CCD n layer as shown in the insert in Figure 1. These electrodes are L_1 in length and separated by a gap length of L_2. The primary parameters of design in a High Speed CCD (HSCCD) are L_1, L_2, the layer thickness T and the layer carrier concentration N. Figure 1 is a general figure which shows in a simple way many of the trade-offs involved in the choices of N and T.

One of the most fundamental constraints the designer must adhere to in designing CCDs is that he produce a device for which the minimum required drive voltage level at the maximum clock frequency be attainable. Presuming that this clock voltage is to be supplied by GaAs FET Integrated Circuitry and that the clock frequency will be 1 GHz, the attainable minimum peak to peak voltage level would be 7 volts. It is a good rule of thumb that the most significant device performance parameters are determined.

A couple of extra lines in the Figure 1 are lines of constant value of $\int n(y)dy=(I)$. This number is the number of free carriers per cm^2 that can be accomodated in the layer. It is a measure of the maximum number of electrons that can be accommodated under an electrode Qm (maximum well charge). Since a large maximum well charge Qm is desirable, it would seem a straight forward choice to choose a layer of high N and lower T. However, there is one very important factor that drives the designer in the opposite direction. This is a quest for speed. The reasons for this are based upon considerations best explained using Figure 2.

In Figure 2, the ordinate represents the time required to clear charge out of one well and place it in another. The time on the ordinate is that time required to move .9999 of the well charge. The abscissa T_0 is the depth of the potential well minimum. This depth is generally less than

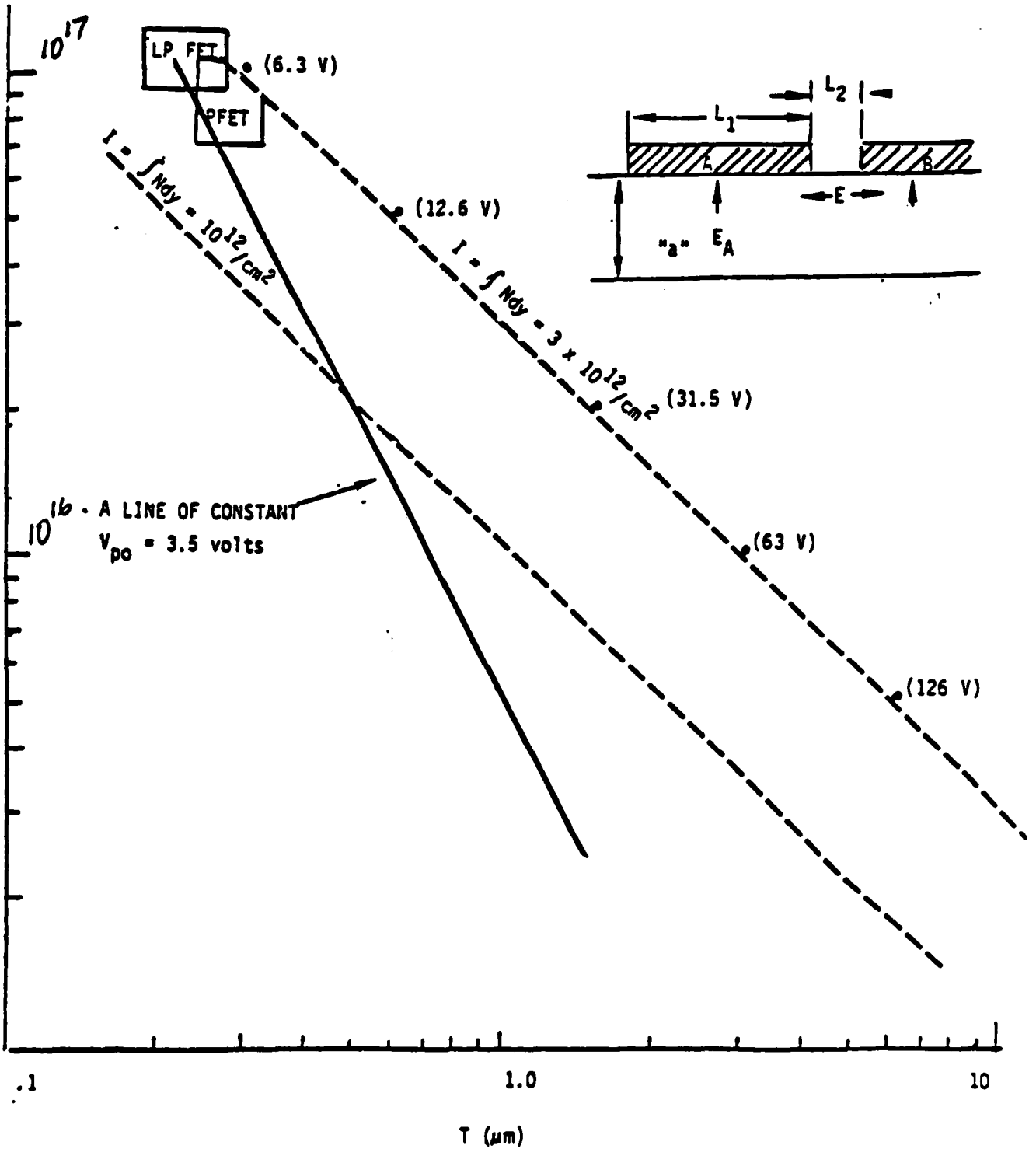


Figure 1. The allowed variation of carrier concentration, N, and active layer thickness T for CCDs and FETs are depicted in a plot of N vs. T. The figures in parentheses represent complete depletion voltages for each combination of N and T.

the active layer thickness but may equal the active layer thickness if the substrate is a material of very high resistivity but with very few background acceptors (assuming it to be p material). For the sake of simplicity, we will assume that To is a fixed fraction of T like 0.99 T. A further piece of information in Figure 2 is the effect of the interelectrode spacing L ($=L_1 + L_2$) upon the time required for charge transfer.

The message of Figure 2 is that to obtain .9999 of the charge transferred at 870 MHz, the minimum T_o is a strong function of L and this dependence is plotted in Figure 3. L is determined by the need to have a reasonable signal level since maximum signal level Qm is proportional to the product of L and W, the electrode width. The electrode width W cannot be very wide because the resultant extra spurious capacitance would be intolerable. Lithographic considerations also play a part and the minimum geometry of lithography, i.e., the gap distance L_2, is going to be about 1 μm. For devices to work at 870 MHz, an electrode length L_1 of 4 μm and an interelectrode spacing of 5 μm seems an optimum choice. This electrode will normally accommodate about 10^6 electrons in a layer where I = $10^{12}/cm^2$ for a 100 μm width. This means from Figure 3 that a T_o value of at least 1.25 μm must be obtained in the CCD active layer. Speed alone dictates this choice of a very thick layer. All other considerations such as maximum signal strength, Qm, ease of fabrication and bulk trapping considerations dictate a thinner, more highly doped layer.

Table 1 has been drawn up to show for uniform profiles how the maximum signal level is compromised as we go to thicker layers and lower doping levels in order to obtain more speed. These calculations are based upon simple uniform profiles and Figure 4 illustrates the model of the layer potential profile and the expressions used. The calculations are done for our electrode size of 4 μm by 100 μm.

In summary, a clocking frequency of 870 MHz calls for a T_o potential well depth of 1.2 μm if the electrode spacing is 5 μm. There is a trade-off between speed and maximum signal charge and at a reasonable pinch-off voltage of 3.5 volts, the maximum signal charge in the 5 μm period CCD (L = 5 μm) is only about 2.5×10^5 electrons. This means a dynamic range

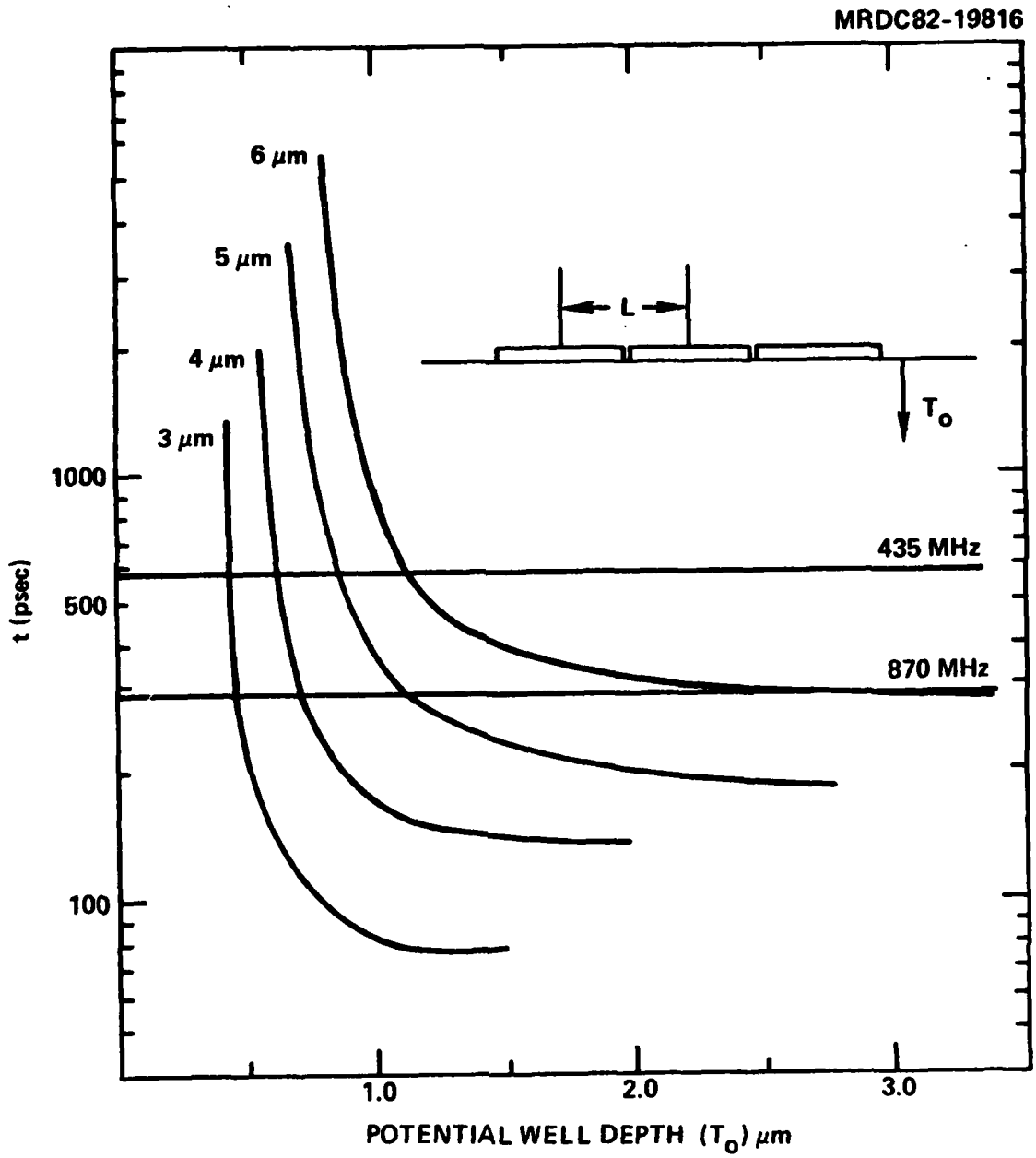


Figure 2. The time required to remove .9999 of the charge from under one electrode and place it under an adjacent electrode is shown as a function of T_o the potential well depth. Also shown is the dependence of this time on the interelectrode distance L.

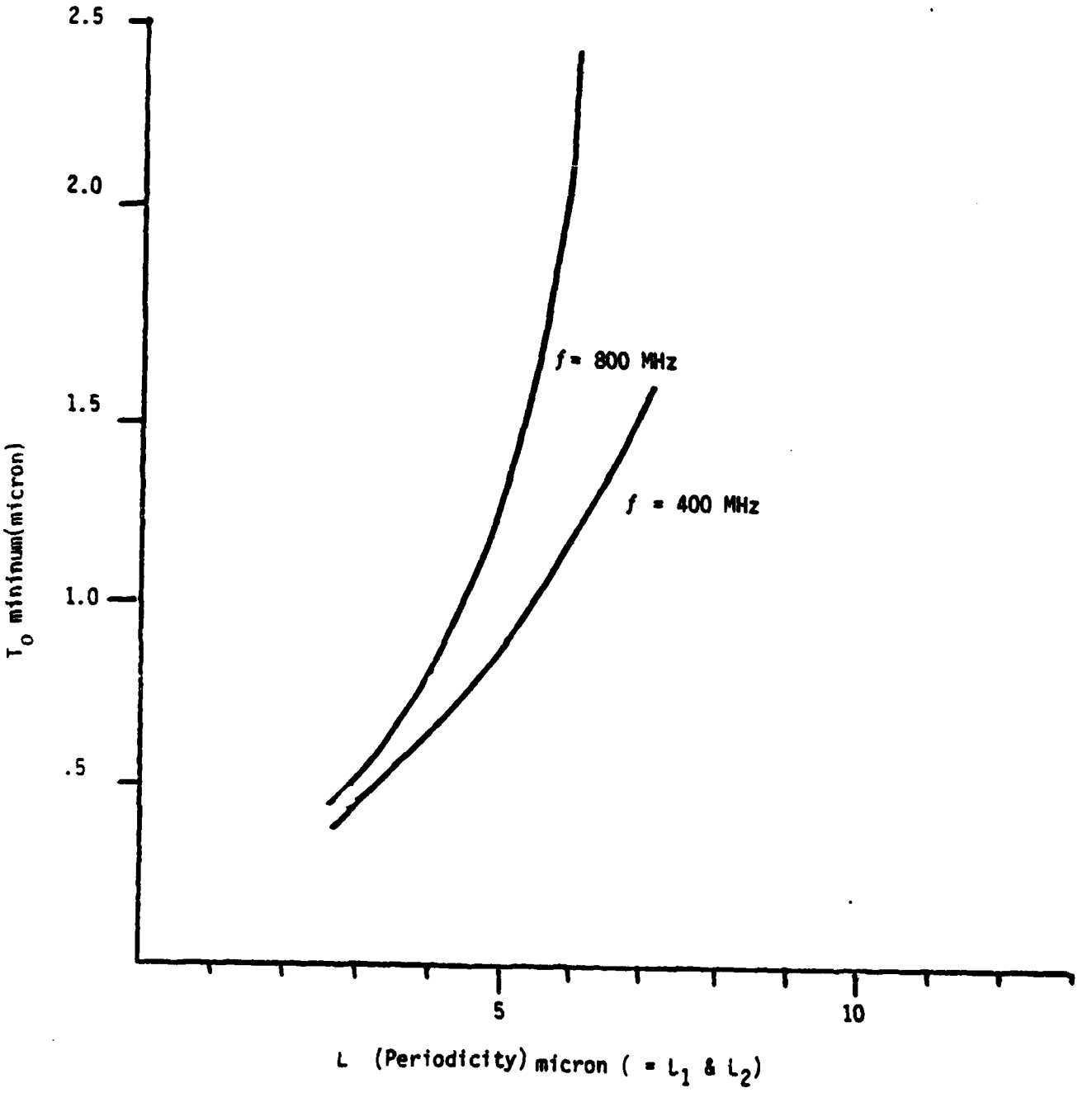
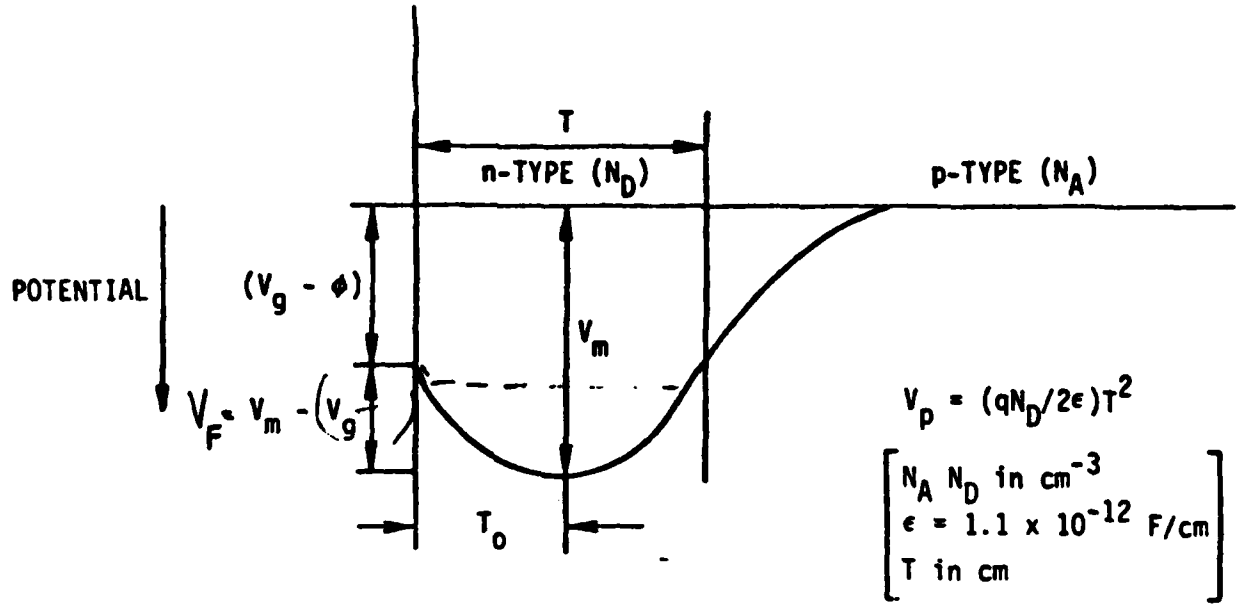


Figure 3. The very sharp dependence of minimum potential well depth upon the periodicity of the gate electrode structure is shown. The criteria for the calculation is the satisfactory removal of .9999 of the charge.

TABLE 1

N/T	T_o μm	f_{max} (CTI = 10^{-4}) L = 5 μm	MAX V DRIVE AT 5×10^5 ELECTRONS PEAK TO PEAK	MAX CHARGE CAPACITY FOR A DRIVE OF 0 V 7.2 V CHARGE CAP.
2×10^{16}/0.5 μm	0.41 μm	150 MHz	> 10	$> 1.25 \times 10^6$
1×10^{16}/0.7 μm	0.54 μm	200 MHz	7.0	5×10^5
5×10^{15}/1.0 μm	0.71 μm	300 MHz	5.0	2.5×10^5

Trade-offs in speed and charge carrying capacity for uniform layer CCDS.



$$\text{FACTOR} = \frac{1}{N_D/N_A}\left[\left(1 + \frac{N_D}{N_A}\right) - \left(1 + \frac{N_D}{N_A} + \frac{N_D}{N_A}\frac{(V_g - \phi)}{V_p}\right)^{1/2}\right]$$

$$T_o = T * \text{FACTOR}$$

$$V_m - (V_g - \phi) = V_p * \text{FACTOR} * \text{FACTOR}$$

FOR A WELL CHANGE OF Q_w, T MUST BE ALTERED TO

$$T = T - (Q_w/qA)/N_D$$

WHERE A IS THE ELECTRODE AREA IN cm^2.

Figure 4. The potential well calculations for the simple case of a uniform layer.

of 30db is the noise floor of the device and is taken to be about 250 electrons, a reasonable assumption.

2.2 Integrability of the CCD

Another aspect of designing these devices is their incorporation upon the GaAs chip with the support circuitry, i.e., they must be incorporated with planar FET GaAs circuitry. The successful high speed use of this device in any application will depend upon this integration because hybrid interconnection of digital circuitry or clock driver circuitry (where the preservation of gigabit waveforms is essential) is not as easy or as economic as full integration. In present CCD programs the most immediate task is integration of sampling pulse generators and clock driving amplifiers. Eventually the clock generation schemes and programmable tapping systems must be incorporated onto a CCD chip.

In this chapter, we discuss the methods available to achieve the deep layers in the context of GaAs FET IC Technology and a justification is presented for the method chosen. Basic to this discussion is the position that the CCD layer cannot be FET-like in that it cannot be highly doped and sub-4000Å in thickness. It must be thick for speed and fairly lightly doped. The methods to be considered (in order of ease of fabrication) are:

A) Direct implant into a substrate
B) Implant into a buffer layer
C) Epitaxial Layer/Mesa etch/Implant FETs
D) Selective epitaxial growth/Implant FETs
E) Epitaxiallayer/O^+ implant/Donor implant

Method A was the method first chosen. We will discuss very briefly here all the methods starting with the least desirable (E). In methods, C through E, the CCD layer is formed by epitaxial growth and the support circuitry is to be installed by implant technology.

E) Oxygen Implant

The objective of oxygen implant is to render semi-insulating the unused epitaxy and thereby provide an area for placing FETs by implant. This is a very complex series of steps and has no precedent. On that basis, it is not considered except in the context of a possible materials research project.

D) Selective Epitaxial Growth

Epitaxial growth in local areas defined in insulator and in etched holes in the GaAs was carried out experimentally in another program and the results were not encouraging. Anneal cycles for subsequent implant of FET devices were also found to affect epitaxial layer profiles. Therefore, this method was not chosen.

C)Epitaxial Layer/Mesa Etch

This method is perhaps the most simple for defining the CCD active layer areas. The FETs of the support circuitry would be implanted into the mesa floor and annealed. The problems of working with topography changes of 1 to 2 μm in height and the changes wrought in epitaxial layer profiles by annealing cycles were considered sufficient reason to avoid this technique.

B) Implant Into Semi-Insulating Buffer and A) Direct Implant Into Melt Grown Semi-Insulating GaAs

These two methods are the most straightforward for arriving at all the different device active layer profiles called for. These were tried in our program. In the early stages (which are the subject of this report) Method A was our exclusive interest and as the results developed, it became apparent that better substrate material was needed and so our attention turned to Method B.

The problems of direct implantation appeared at the outset to be primarily concerned with obtaining sufficient energy for the implanted ion (Si) in order to get to 1 μm projected range. We could at the Rockwell implant facility attain an energy of 750 KeV; but to get to a range greater than 1 μm, an energy of 1 MeV to 1.5 MeV would be necessary. To attain this, it was necessary to have the implants done by RADC Hanscom AFB. This reduced the number of implants that could be achieved within the time interval of the program.

In Figure 5, the process of integrating a CCD into regular GaAs FET IC is depicted. An all implant process carries the greatest simplicity and as emphasized by this figure, provides the planar surface so important to yield considerations in Integrated Circuitry. In the interests of trying the process, it was decided to make CCDs implanting silicon ions at energies of 750 KeV and 1 MeV. Even though these would not provide (by our calculations) CTE of .9999 at 870 MHz, they would do so in the 400 to 500 MHz range. The 750 KeV implants were obtained by using doubly ionized silicon in the Rockwell accelerator and the 1 MeV singly ionized silicon implants were performed at RADC.

A further compromise in this program for implanted layers is evident in the fact that we allowed the pinch-off voltage to rise slightly. This was done in the interests of having higher peak carrier concentration and a larger charge package in the devices. This would give a larger dynamic range and make the devices more immune to bulk trapping effects at the cost of requiring more drive power in the clocks. Table 2 gives the details of the expected layer characteristics for an implant dose of 1.25 x 10^{12} silicon ions/cm^2. For ion implantation, the profile is not a uniform profile but rather a Gaussian profile as shown in Figure 6. This figure depicts the expected profile from our implant experiments for the above stated dose.

In summary, the approach primarily in this program was to obtain an active layer for the integrable CCD by direct implantation on a localized basis. The energy chosen and the dose chosen were such as to obtain a layer with a shallower T_o and a higher pinch-off voltage than are ideal.

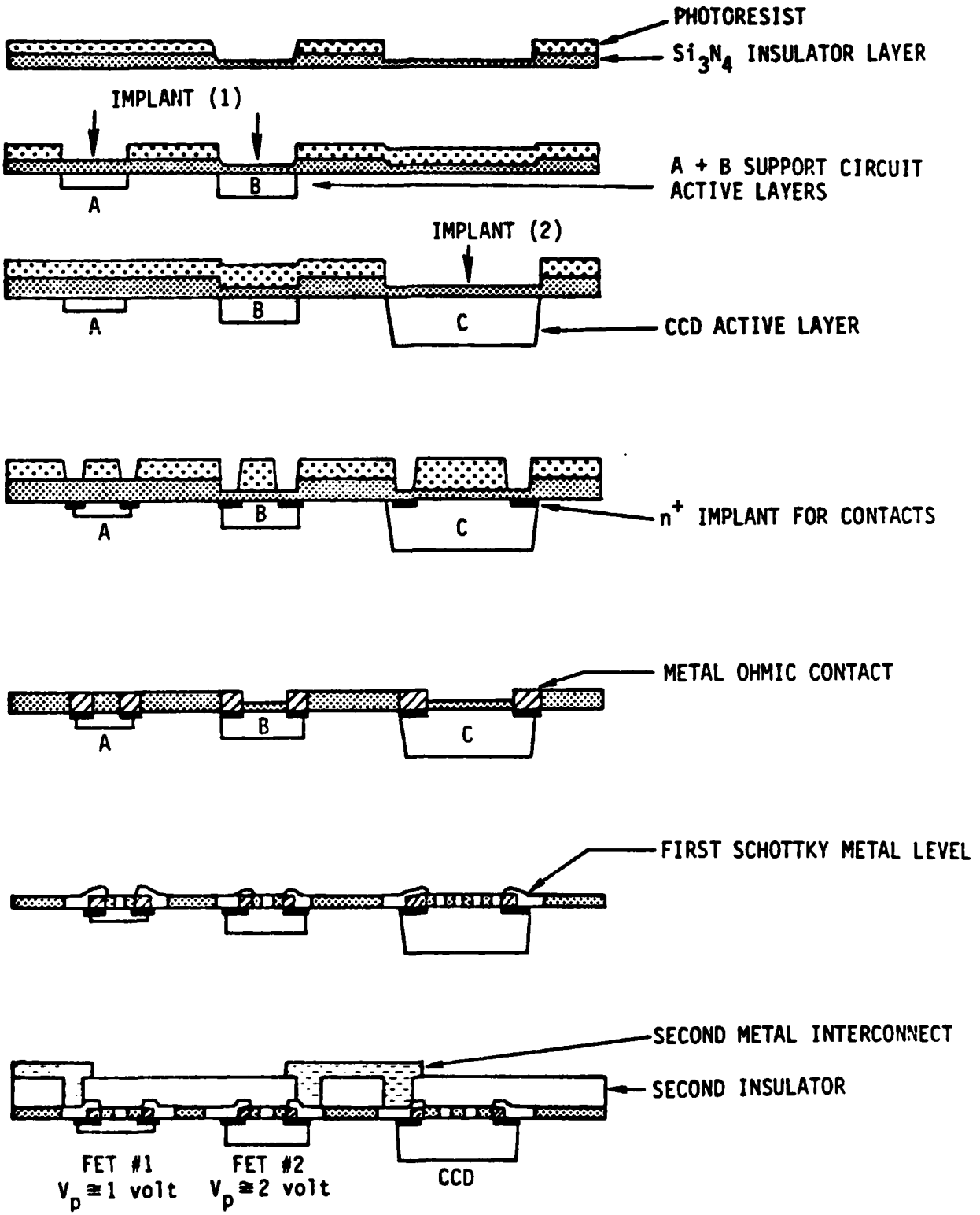


Figure 5. The fabrication process

TABLE 2

Calculations of Pinch-Off Voltage And Range
For Implant of 1.25 E12/cm^2 Silicon Ions

Energy KeV	Nitride Thickness (μm)	Layer Thickness (μm)	T_o or R_p (μm)	Pinch-off Voltage (V)
1000	0	1.15	0.82	8.2
800	0	0.98	0.675	6.56
1000	0.05	1.1	0.77	7.6
800	0.05	0.93	0.625	5.99

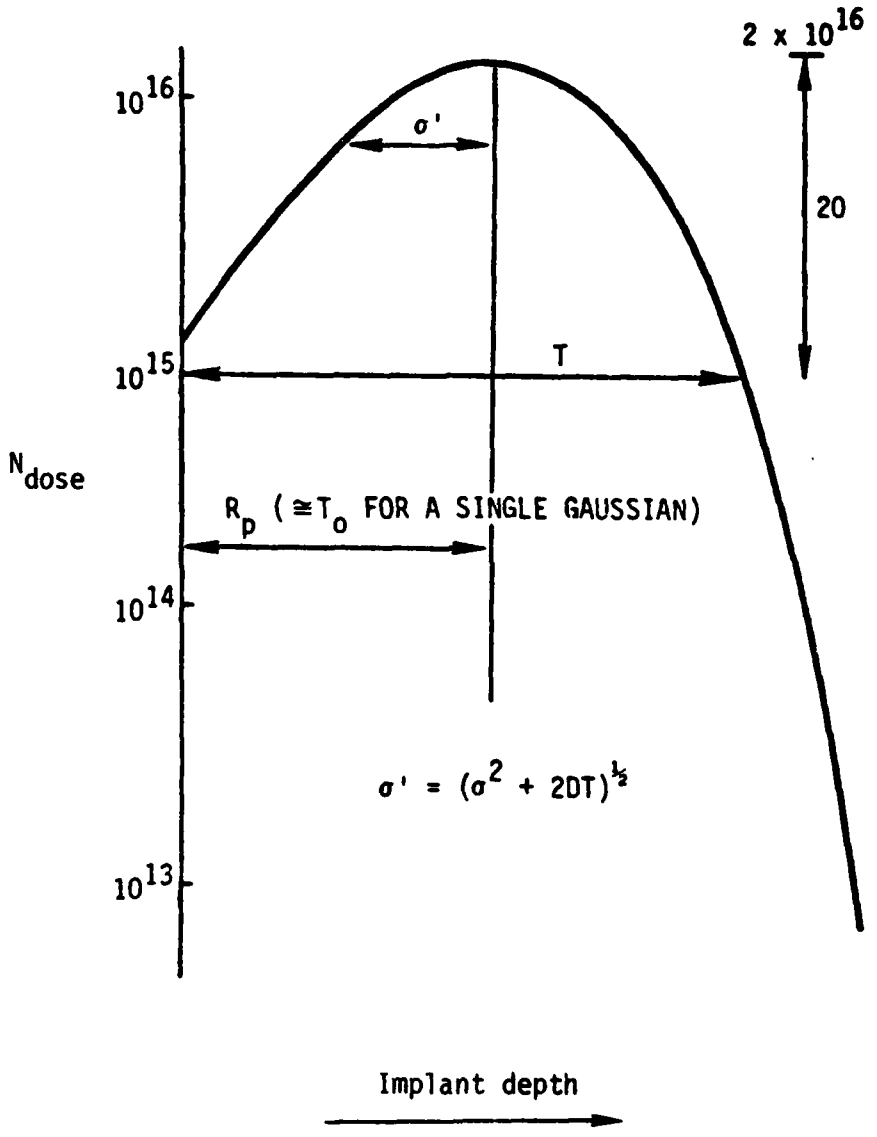


Figure 6. A Gaussian doping profile such as may result from a single dose ion implant. The total thickness, T, is approximately $R_p + 1.73\,\sigma'$. For a ξ = 1000, R_p = 0.83, σ = 0.19, T = 1.15μm; for ξ = 800, R_p = 0.675, σ = 0.178, T = 0.98μm. R = R_{GaAs} - Si_3N_4 thickness.

Chosen energy and dose: - 750 KeV and 1000 KeV
1.25 E12/cm^2 (assuming 90% activity)

Expected T_o and Vp: T_o = .67 and .77 μm
V_p = 6 and 7.5 volts

Ideal for high speed CCD T_o = 1 to 2 μm

$V_p \cong$ 3.5 volts

The compromises, therefore, meant a slightly shallower layer than desired and a higher pinch-off voltage. The reasons for accepting these are both practicality and a higher carrier level which meant more immunity from bulk trapping effects and a better chance of being above the compensation effects probably present in the bulk crystal.

2.3 Near Surface Implantation

A consistent matter of concern in designing layers for CCD devices is the matter of the trade-off that is evident between dynamic range and possible device speed. This trade off is straight forward or uniform layers being a matter of selecting N and T as indicated in a previous section. But when layer design can be more sophisticated and the layer may be non-uniform then some additional complexity in the layer design can lead to an increased dynamic range and high speed simultaneously. The layer profile of Figure 7 is an example of just such a layer design. The implantation of a deep peak of donors to ensure the potential well minimum is deep (in the layer) is accomplished by a high energy implantation ($\cong$ 1 MeV). Then an extra implantation of donors at a shallow depth near the surface to provide more charge storage capability is done. Since this extra charge is placed near the surface, it will not contribute substantially to pinch-off voltages. A double peaked implant such as this would provide both a deep potential minimum and enhanced charge capacity (Qm) thus improving the overall capability of a CCD.

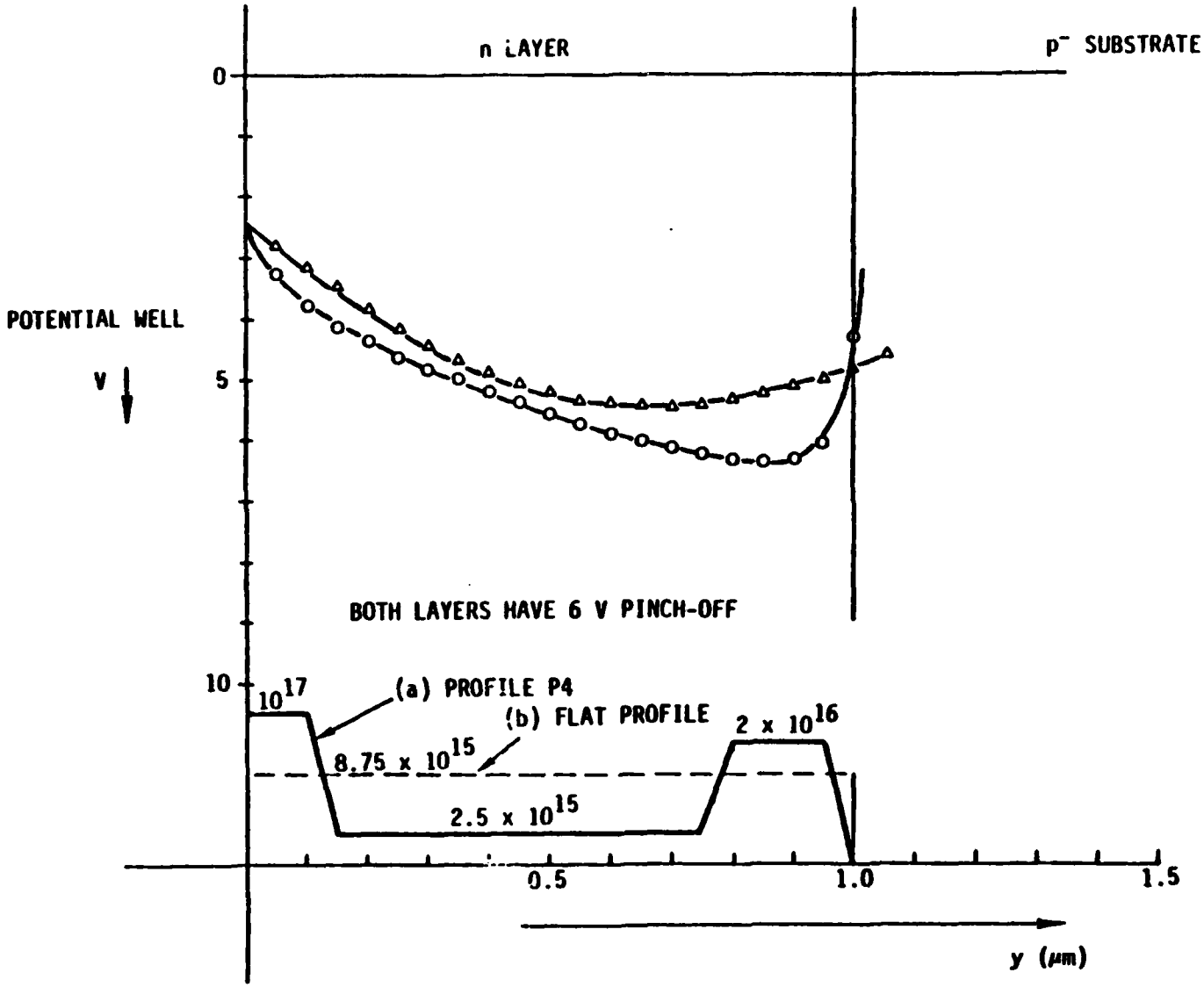


Figure 7. A complex profile including a deep peak for speed of transfer and a shallow peak for extra charge carrying capacity.

Some of the wafers sent for high energy implant also received this surface implant and the results in as far as layer activation was concerned were encouraging. Device behavior, however, was dominated by what appeared to be bulk trapping effects.

2.4 Experimental Results

It is an absolute necessity to characterize as thoroughly as possible the starting material in implanting GaAs. This is especially important in the case where the implanted dose levels are as low as 1 to 2 x 10^{12} ions/cm^2. Qualification of boules of semi-insulating material is accomplished by a set of procedures [1] based upon the needs of FET devices where the carrier concentration levels are $10^{17}/cm^3$. These procedures were applied to the material used for this program and only material which passed this strict testing was used. Experience from these low dose implants indicates that (as might be expected) the impurity levels in the starting materials can be much more significant in their effects on layers where the intended doping level is in the low $10^{16}/cm^3$. These effects are variability of the actual resulting carrier concentration levels from wafer to wafer and within a wafer.

The procedures for boule qualifications are well known by this time having received quite wide publicity [1,2]. They are based upon the need (as mentioned above) to achieve implanted peak doping levels of $10^{17}/cm^3$. As a result of this qualification, it became apparent that the activation level dropped from the 90% normally encountered. To achieve a profile of 2 x $10^{16}/cm^3$ peak took more than the calculated dose of 1.25 x $10^{12}/cm^2$ which is based on the 90% activation normally achieved with FET implants (peak = $10^{17}cm^3$).

In general with the boules used in the early experiments, a dose level around 1.65 x $10^{12}/cm^2$ was necessary indicating activation reduced to the level 65% to 70%. This is easily reconcilable with a model where

background impurities of deep acceptor levels are a fixed quantity and make a proportionately lower fraction of the higher doped layer. From simple calculation, it appears that 0.3 to 0.5 x 10^{12} implanted ions fill up the background impurity level.

In Table 3 (which is for samples sent to RADC for 1 MeV implants), it is indicated that for batches 2 through 5 the specification of dose on the level 1.65 x 10^{12} led to pinch-off voltages that were too high: i.e., > 7 volts. This anomolous difference between expected and actual results is difficult to explain especially since the doses were prescribed on the basis of qualification of test implantation done on pieces from the same boule. Batches 1 and 6 behaved nicely according to expectations. It is to be noted that batch 6 was implanted with a reduced dose. This was due to the results received from the qualification test implant which indicated that the dose should be low. The one conclusion that can be drawn from the table for the 1 MeV implants is that there is an intolerable amount of non-uniformity in the wafer pinch-off voltages in all cases. The non-uniformity is above the 10% upper limit normally tolerated in FET layers and goes up to 50%.

Another factor to be considered is depicted in a final column of the table showing the number of wafers that showed little or no activation. It is not clear at present whether this was a machine problem or not. If so, it is peculiar that chrome doped samples were particularly unlucky in this respect. We suspect that there is a need for more research in this area and that chrome doped layers have a higher background density of impurities together with more complication due to movement of the Cr atoms.

In Figure 8, we show the profile from a wafer from batch 4 revealing an ideal profile with which to fabricate a CCD. The situation would be even closer to ideal had the implants activated uniformly over the entire area of the wafer. However in general, this is not the case as evidenced by the wafer map of a batch 6 wafer shown in Figure 9.

Figure 10 shows the type of profile generally obtained using the Rockwell implantation facility. A profile of usually lower projected range, it is obtained with better control over its variation over the wafer. The

TABLE 3

HIGH ENERGY IMPLANTS FROM RADC

BATCH	BOULE	NO. OF WAFERS	ENERGY	DOSE	V_p	σV_p	NO ACT.
1	UNDOPED C	12	1 MeV	1.65×10^{12}	4.86	1.86	25%
2	UNDOPED B	2	1 MeV	1.65×10^{12}	14.00	4.00	0%
3	Cr DOPED B	6	1 MeV	1.65×10^{12}	12.00	6.00	50%
4	UNDOPED C R-28	10	1 MeV	2.00×10^{12} 1.5×10^{12}	11.00 7.00	5.00 3.00	0% 0%
5	Cr DOPED C	2	1 MeV	1.5×10^{12}			100%
6	UNDOPED C R-29	5	1 MeV	1.25×10^{12} 1.00×10^{12}	4.26	1.99	20%

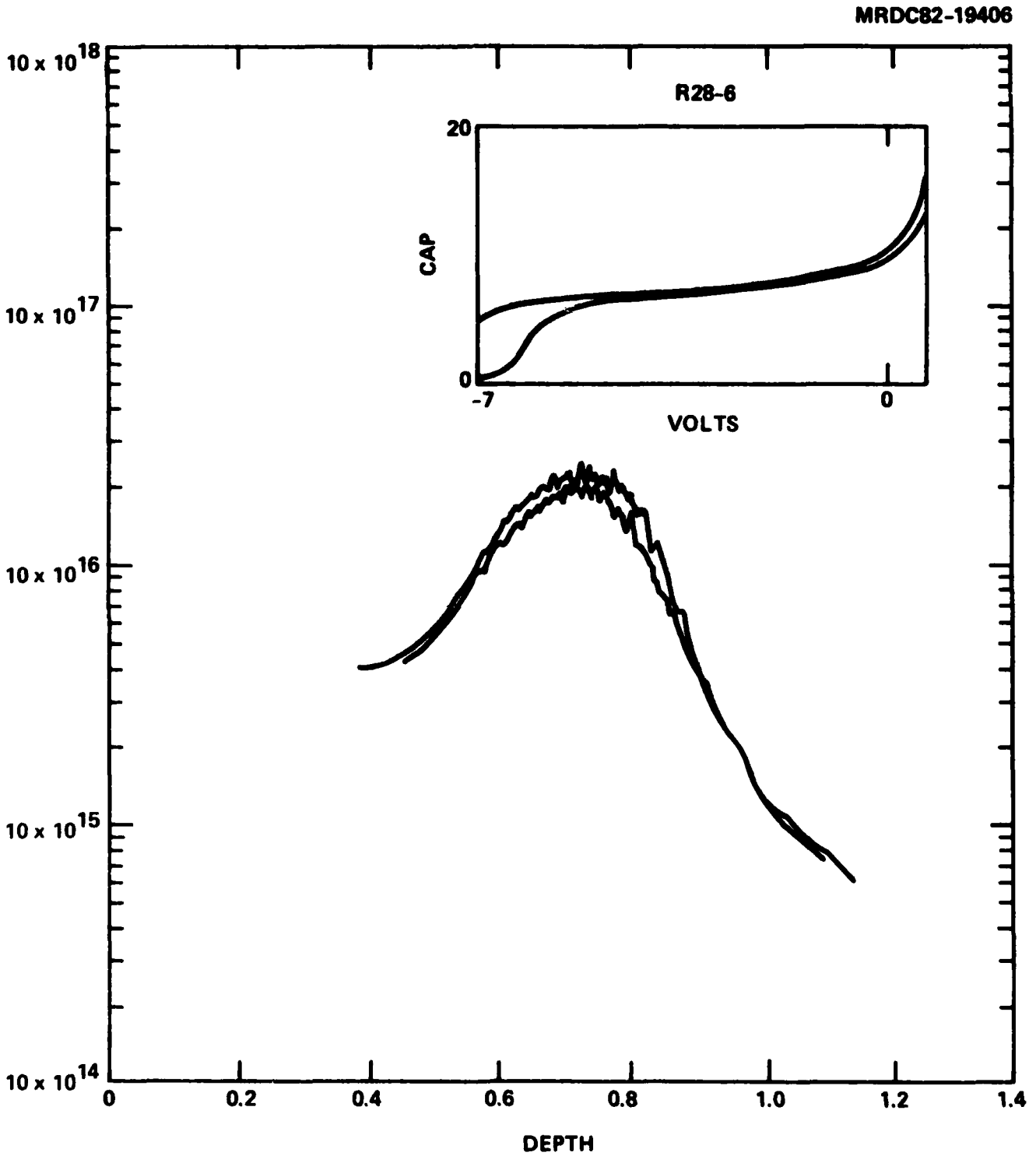


Figure 8. Example profile from the lower dose implant of Batch 4 (See Table 3) 1 MeV implant RADC.

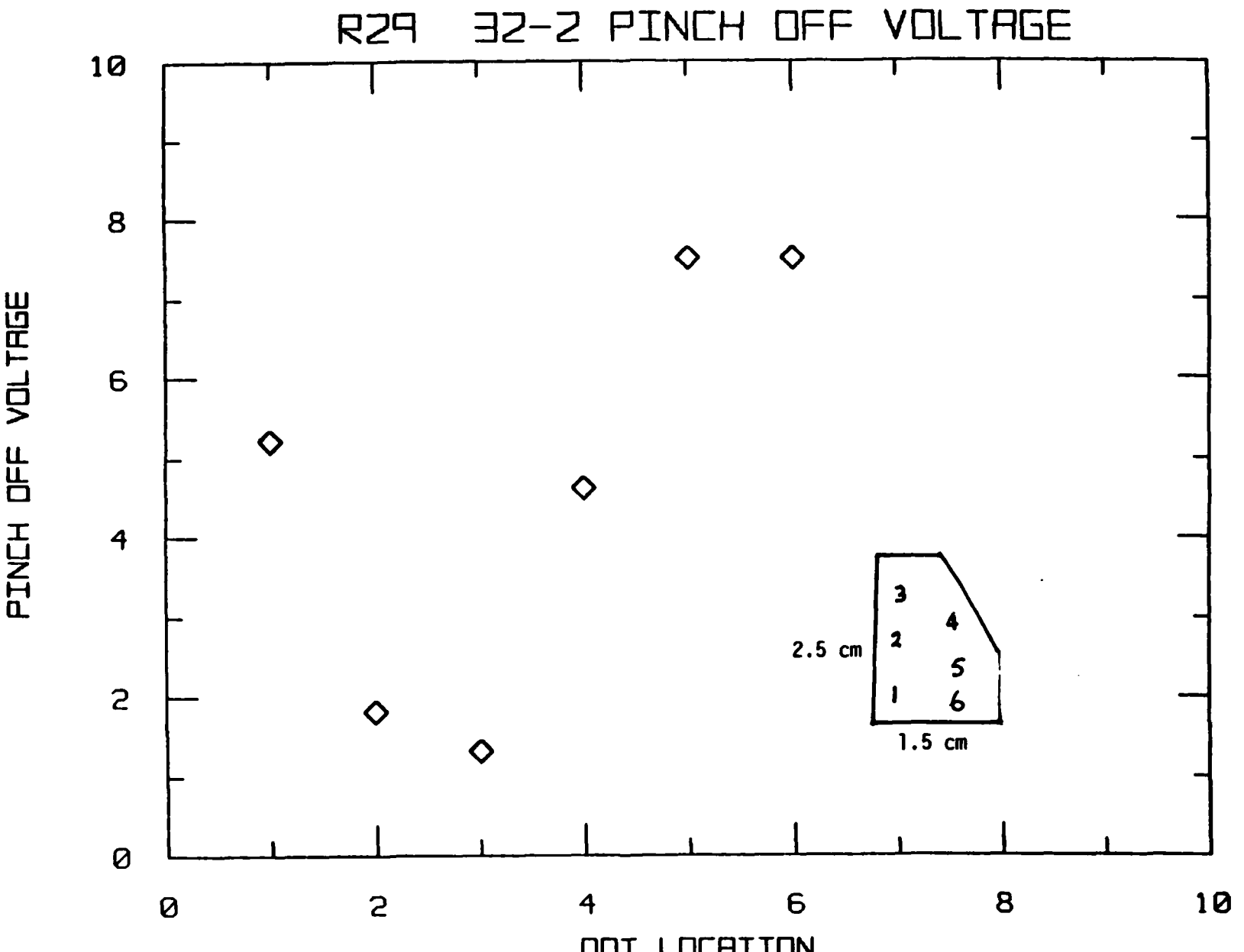


Figure 9. An example of the variation of pinch-off voltage over a wafer which had a 1 MeV implant.

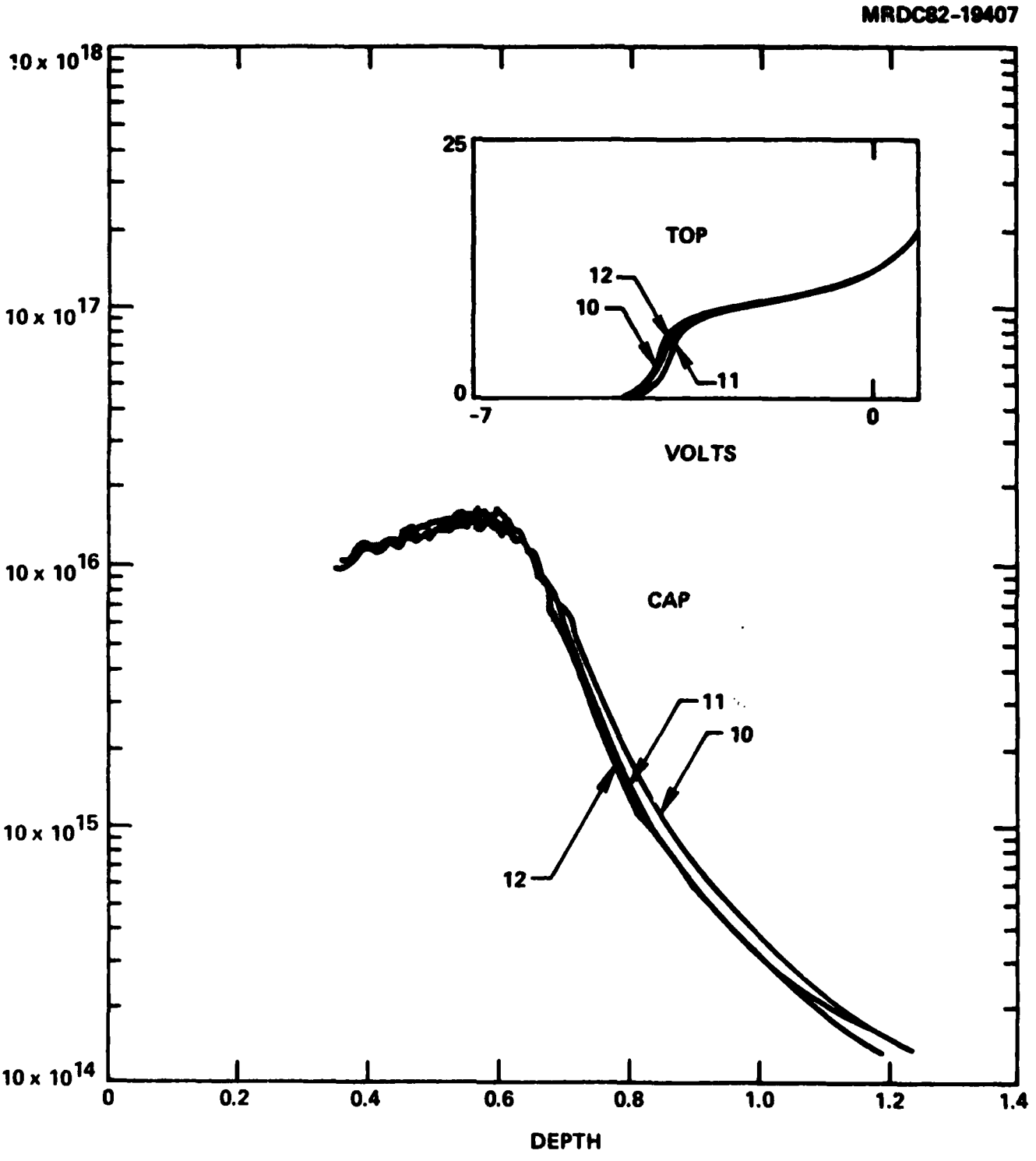


Figure 10. Shallower layers which are the result of doubly ionized implant of Silcion at 375 KeV.

figure illustrates the superposition of the profiles from three widely separated spots on a 1 inch wafer in its longest dimension. Figure 11 contrasts the pinch-off variations of an inhouse implant over the length of device and the pinch off variation of one of the deeper more lightly doped layers.

Finally Figure 12 shows a profile that results from an RADC implant which was then followed by an inhouse implant near the surface. The 1 MeV implant was from batch 1 and before annealing a second implant of 1 x $10^{12}/cm^2$ of 100 KeV Si^+ ions was performed. The resulting profile is one which was expected to give high frequency CCD operation with enhanced dynamic range.

2.5 Device Operation

Devices were fabricated using the HSCCD mask set on implanted wafers. These devices are 32 bit and 64 bit CCDs on a four phase system. In Figure 13 some of the devices in the wafer are shown.

Preliminary wafer probe measurements of these devices have indicated that the charge transfer is bad even at very low frequencies. The suspected reason for this has been narrowed to bulk trapping problems in the implanted layers. Figure 14 shows the response of a 64 bit device with a 6 μm periodicity. The charge packet of 3 pulses has been smeared out completely ruining the CCD action.

Confirmation of the presence of trapping effects is available from the basic makeup of the undoped semi-insulating materials. It was found by subsequent DLTS measurements that the concentration of a trap known as EL2 (an electron trap with a long time constant) is about 10^{16} cm^3 in the undoped Czochralski semi-insulating crystals. This trap would survive the implant process. Also, it is probable that the number of trapping centers is enhanced by the implant process itself.

Subsequent plans now are emphasizing the hot implants of silicon in VPE buffer layers (Method B). This appears to be the best possibility for obtaining implanted GaAs CCDs. These devices shall employ pocket implantation in an integrated circuit as seen in Figure 15. But for quick

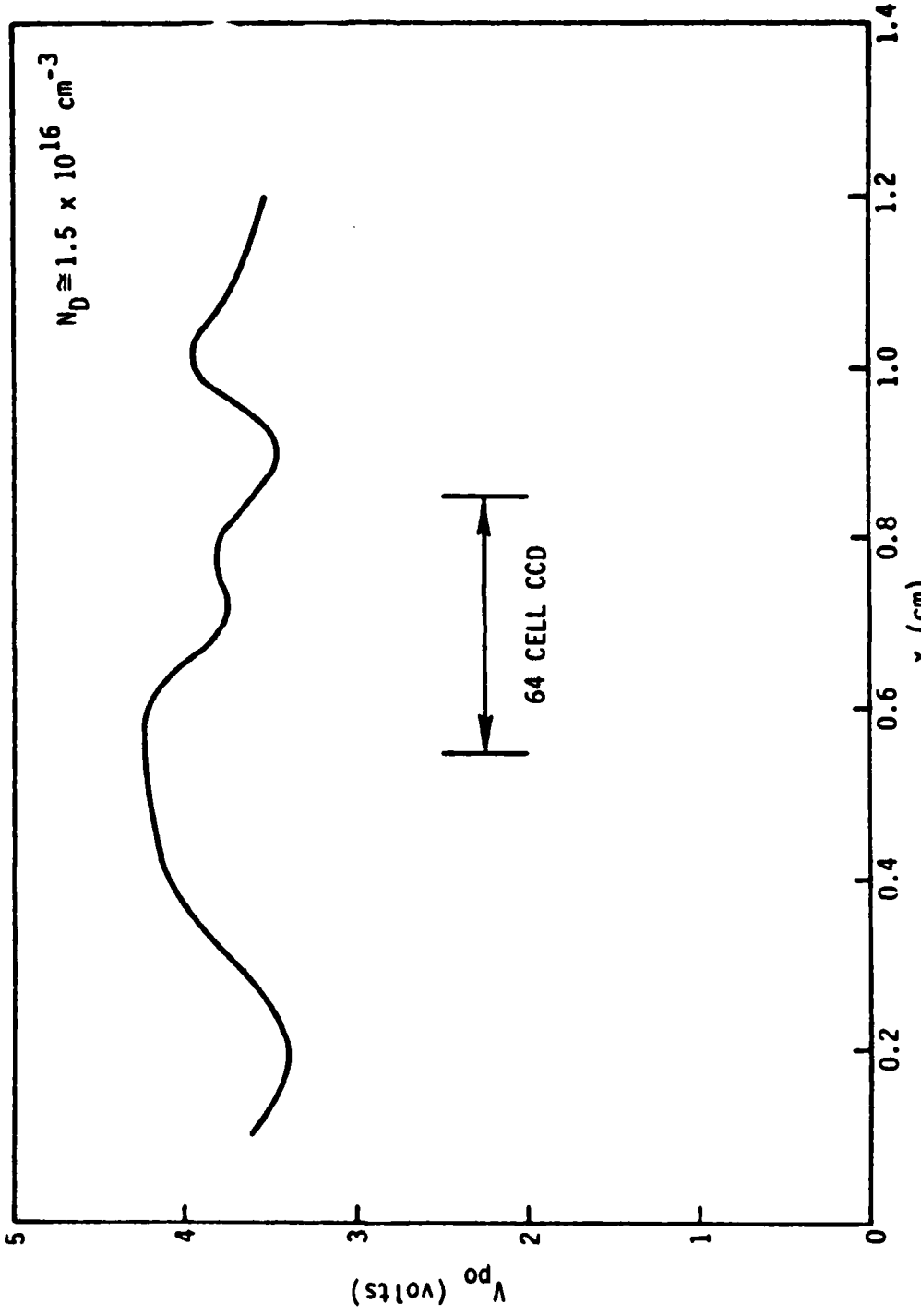


Figure 11. The uniformity of the doubly ionized silicon implants was fairly tolerable although still far from ideal.

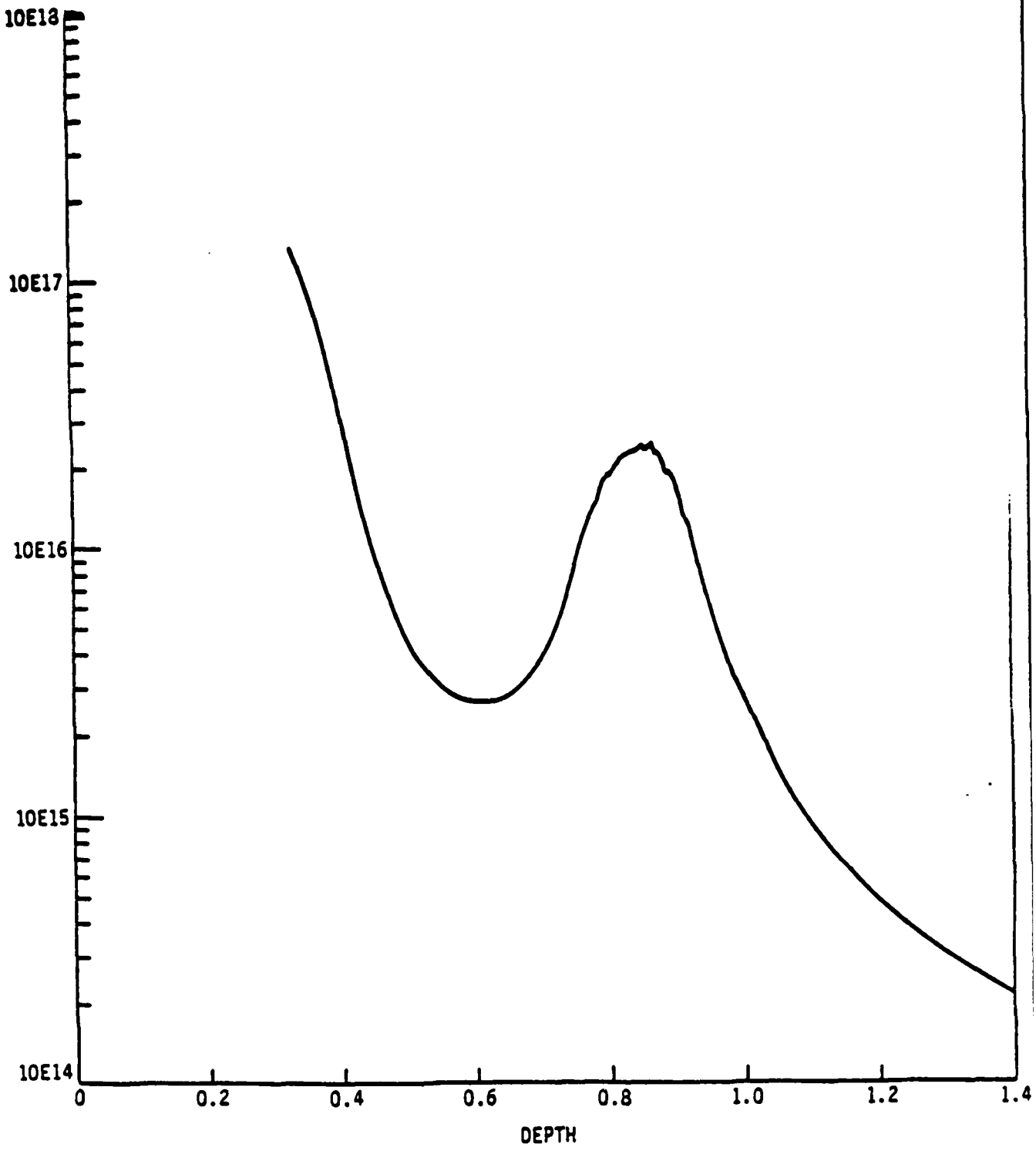


Figure 12. An example of a more complex layer actually achieved by implant.

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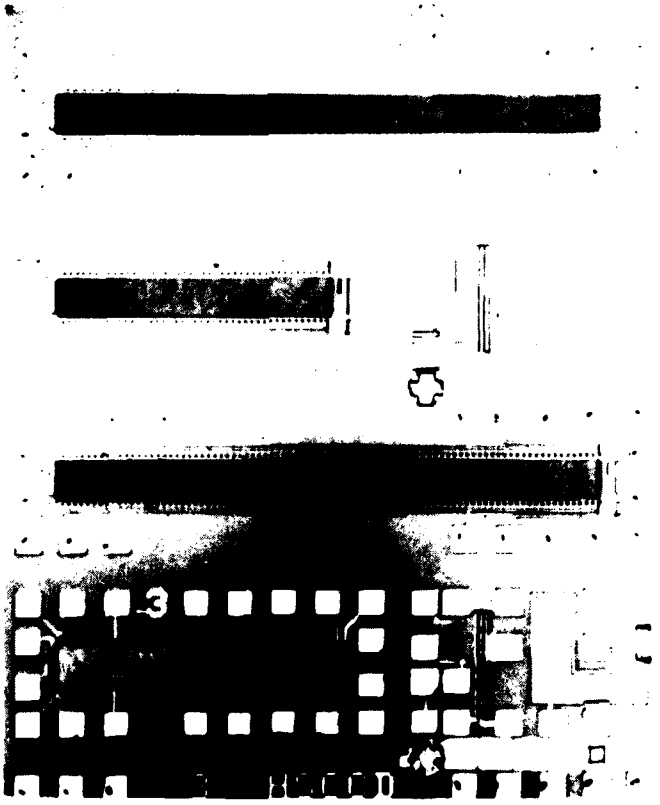

Fig. 13 High speed CCDs fabricated on an implanted wafer. CCDs of three different values of L6, 4.5 and 3 μm are present on this wafer.

MRDC82-18688

CCD OUTPUT

INPUT SIGNAL

64 cell device
259 transfers
Clock Frequency: 625 KHz
6 μm spacing

Fig. 14 Output signal of ion implanted CCDs indicated severe bulk trapping problems.

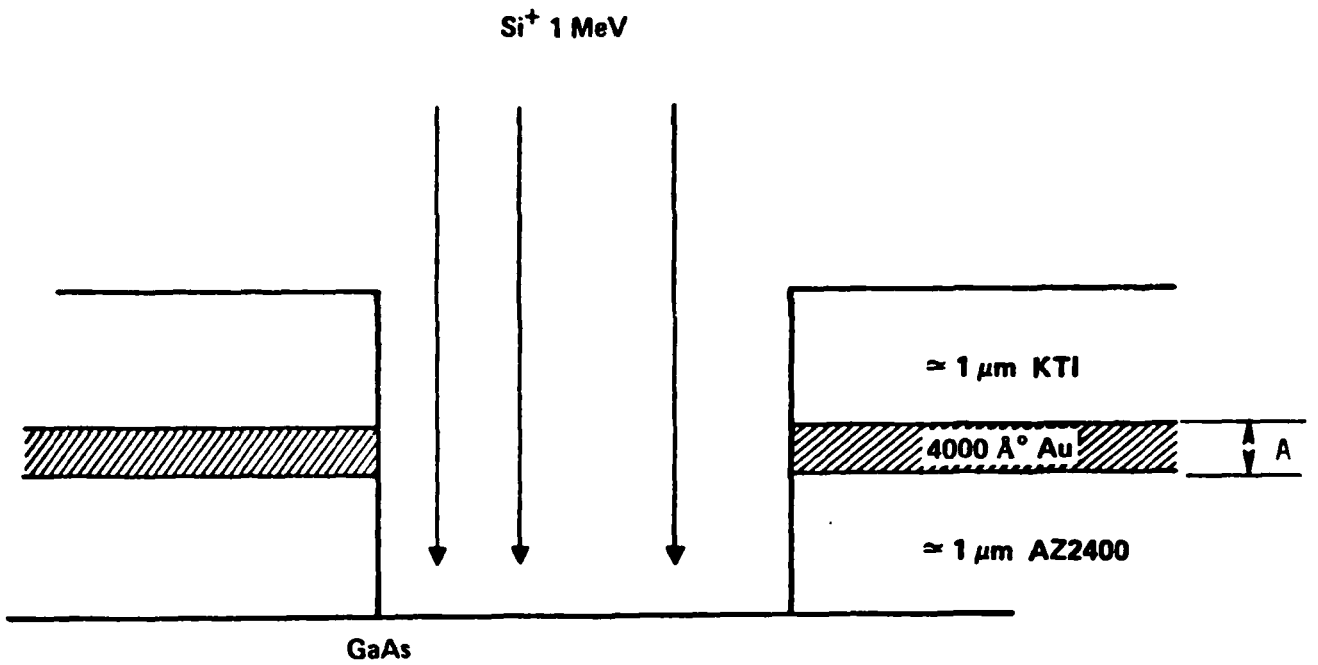

Figure 15. The masking system in use for localized implant and for proton bombardment. A - the gold thickness is 4000Å for H^+ and 1000Å for Si^+ implant.

device evaluation the "all over" implant followed by proton bombardment of areas meant to be semi-insulating shall be employed.

3.0 CCD SUPPORT CIRCUITRY

3.1 Support Circuitry Objectives

In the high speed CCD, a four phase clocking system is employed because it is the clocking arrangement which is least dependent upon the exact shape of the clocking waveform pulse. In the event that a non-square or sinusoidal clock is supplied, the four phase system still functions respectably well. However, the ideal waveform, i.e., the square wave clock pulse ensures the top performance of a high speed CCD. Therefore, a principal task of the support circuits effort was to ensure that the clock waveforms, other sampling and reset pulses, as well as the sampled signal (pulses) are produced with the utmost fidelity. This means care must be taken to design circuits of sufficient bandwidth and phase linearity to perform satisfactorily and that these circuits could be connected together in such a manner as to avoid ringing and loss of proper timing which would also cause difficult problems in testing.

The connections made to a CCD being driven as a simple delay line are shown in Figure 16. This figure also shows that the clock voltages imposed are square waves of peak-to-peak magnitude about twice the active layer pinch-off voltage. The nominal pinch-off voltage is designed to be about 3.5 volts in our devices as discussed in Chapter 2. Reset pulses are necessary at the output to reset the output FET gate and a sampling pulse is necessary at the input to allow charge to flow into the electrode G_2 from the ohmic contact I. All the clock square waves must be maintained in the correct phase relationship between each other and the sampling and reset pulses must be timed correctly with respect to the clock phases. These stringent demands are made to ensure proper device operation and in addition, we want clock frequency to be variable over a moderate range of frequencies, e.g., 500 MHz to 1000 MHz.

The dashed line in Figure 16 represents the package boundary of the CCD under test. It is assumed that the CCD chip is mounted in a package (such as a chip carrier) which will be free of problems of ringing at the frequency range around 1 GHz. This is accomplished by keeping all interconnection lines as short as possible and by design of the test fixture such that the use of controlled impedance transmission lines which may be terminated

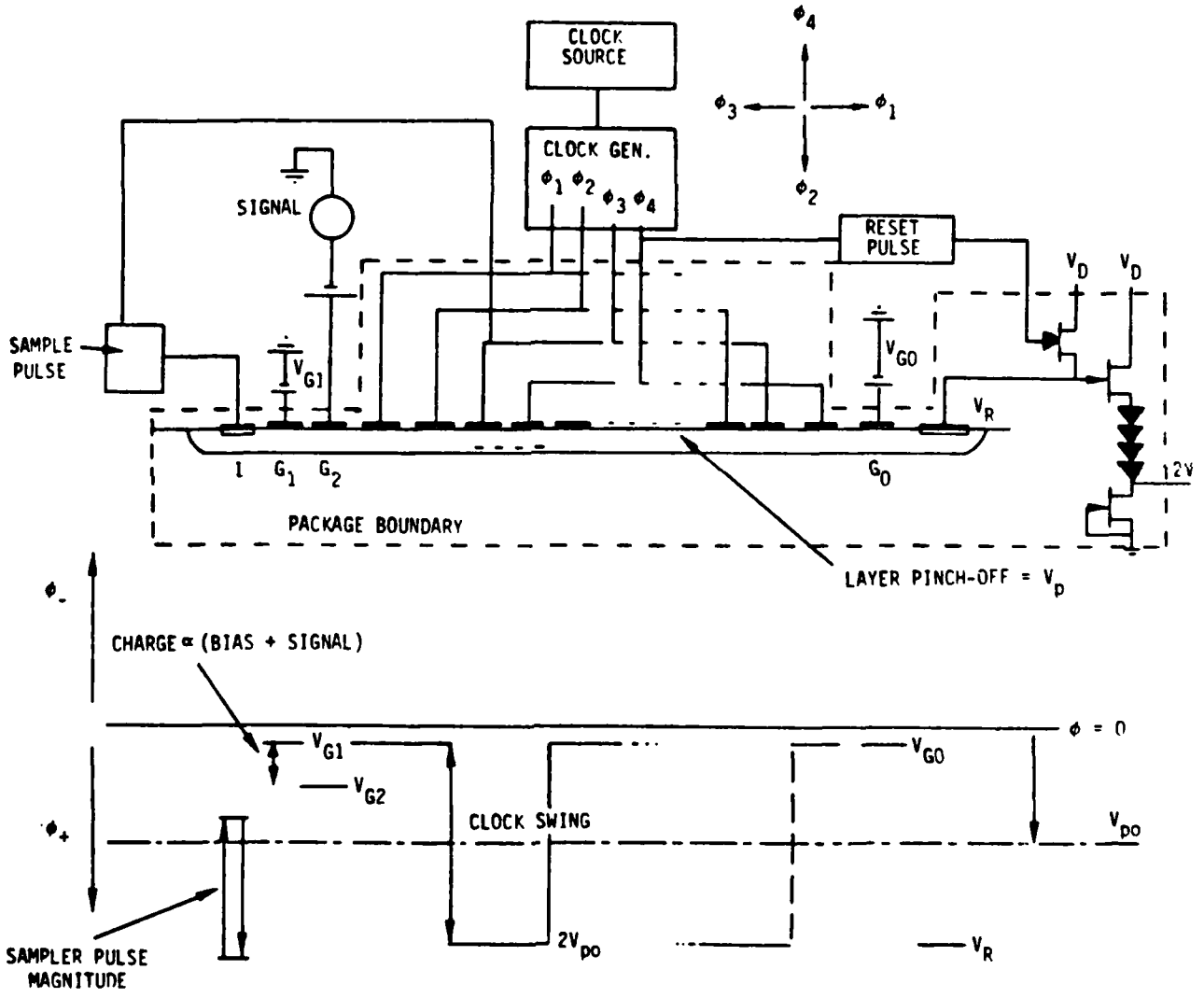

Figure 16. Levels and connections for a CCD under test as a delay line.

for matching purposes is possible. In summary, for the test fixture, the watchword is to keep interconnections short and terminated where necessary. In Figure 17, we have illustrated the probable form of a final test fixture. A hybrid MIC (microwave integrated circuit) approach is taken to interconnect the CCD under test to the output parts of the clock driver chips, fabricated from GaAs FET technology. In Figure 17, only the clock circuits of the delay line test are shown, but in Figure 18 in a more schematic manner, the entire contents of the planned high speed test fixture are shown with some added detail of the methods of clock phase generation.

In Figure 18, some of the blocks representing circuits performing functions are marked with a N. These blocks are the Nonlinear circuits, i.e., those that are digital in function. These digital functions have been designed using SDFL GaAs FET logic circuitry. The principal components are in the clock generation chip which contain all functions within the dashed line in the Figure. A VCO is to be supplied as an alternative to supplying an external source of 2 GHz signal which will provide a 1 GHz clock. This 2 GHz signal is fed to the $\overline{QQ}$ complementary clock generator which is essentially a differential amplifier and clipper. The output from the complementary clock generator drives two flip-flop (divide-by-two) circuits designed to use dual gate FETs in an OR/NAND configuration. The manner of the interconnection of the flip-flops (in parallel but phase reversed) will provide the four 1 GHz clock signals in the proper phase quadrature automatically. All four of the clock signals are fed to the clock electrodes through clock driver circuits which provide a power boost and, if desired, a certain amount of clipping or pulse shaping. The clock driver circuits (CD) and the output amplifiers (O/P) are to be accomplished using the buffered FET or source follower FET circuit approach. This is because that method of FET dc amplifier construction is most suited to obtaining the widest bandwidth with good phase response. We are really using this form of circuit design as a linear amplifier to provide power boost with a minimum of degradation of the waveform. Four separate CD

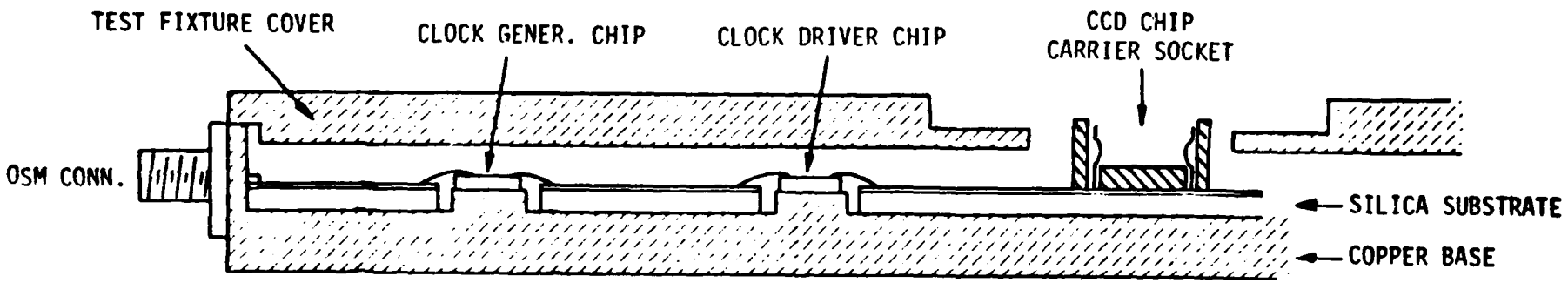

Figure 17. The MIC format to be used for the high speed CCD test fixture.

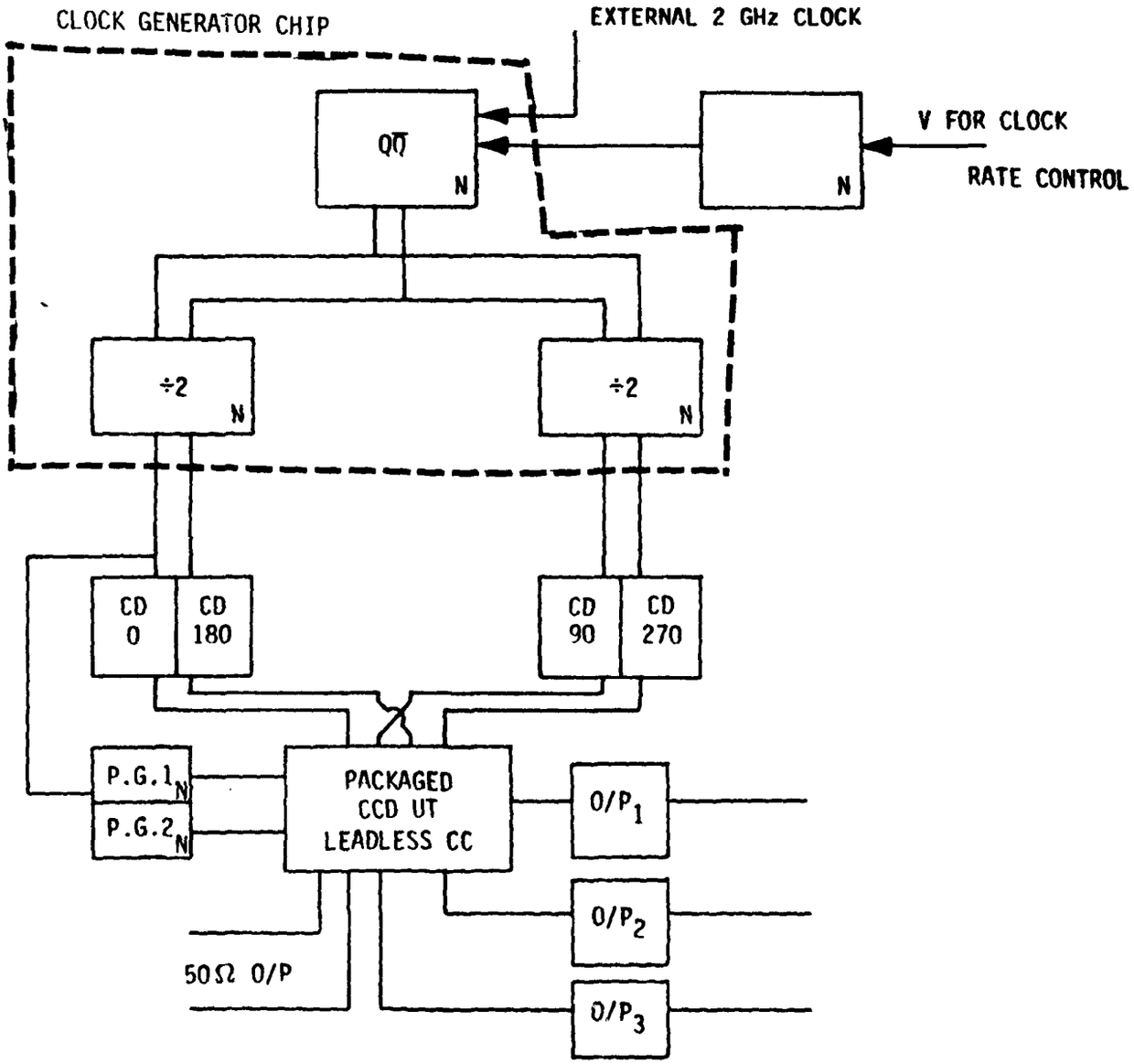

Figure 18. Block schematic diagram of the high speed test fixture

clock boosters and three amplifiers are envisioned on each test fixture. The support circuitry was designed for these specific circuit functions: clock generation, clock power amplifiers and pulse generators or pulse shapers. The designed circuitry was incorporated into a mask set named RA-1.

3.2 Circuit Development

Many aspects of the support circuit mask set (RA-1) are quite new and interesting approaches to the task at hand. They provide prototype elements toward the day when support circuitry and the CCD are fabricated together on the one chip.

3.2.1 Pulse Shaper

As shown in Figure 19, the pulse generators, necessary for sampling and the reset functions at the input and output respectively are based upon SDFL gate strings. We may produce pulses which are integral multiples in duration of the gate stage delay by the use of simple NOR circuits. The numbers inside the symbols show the width of the switching transistor in each case and with the widths shown, τ the stage delay shall be approximately 100 to 120 psec. The circuits placed in the mask set RA1 can be selected by wire-bonding at the final stages of set-up to provide pulses of 360 to 600 psec which should be just fine for clock frequencies ranging from 500 MHz to 1000 MHz. Figure 19 shows the principal involved in these circuits which constitute a simple and effective use of SDFL circuitry to achieve a useful purpose.

3.2.2 Clock Driver Circuits

The schematic diagram of the monolithic clock driver circuit incorporated in mask set RA-1 is shown in Figure 20. It is called buffered FET circuitry because of the use of a source follower connected to the drain node of each amplifying FET. This provides a method of coupling out of the node while providing a high impedance low capacitance load. The placing of the level shifting diodes in the source follower circuit

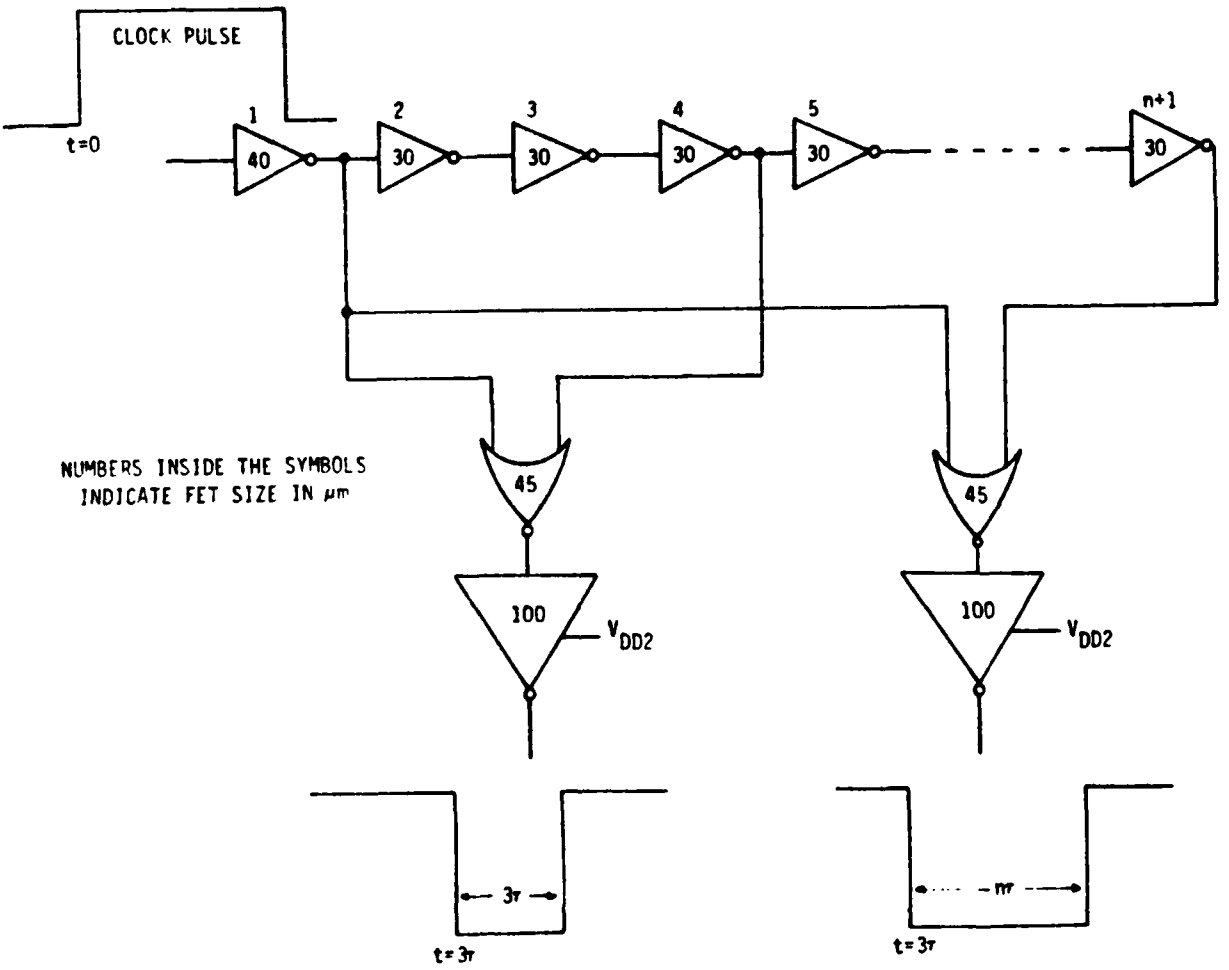

Figure 19. Block schematic diagram of a pulse generator.

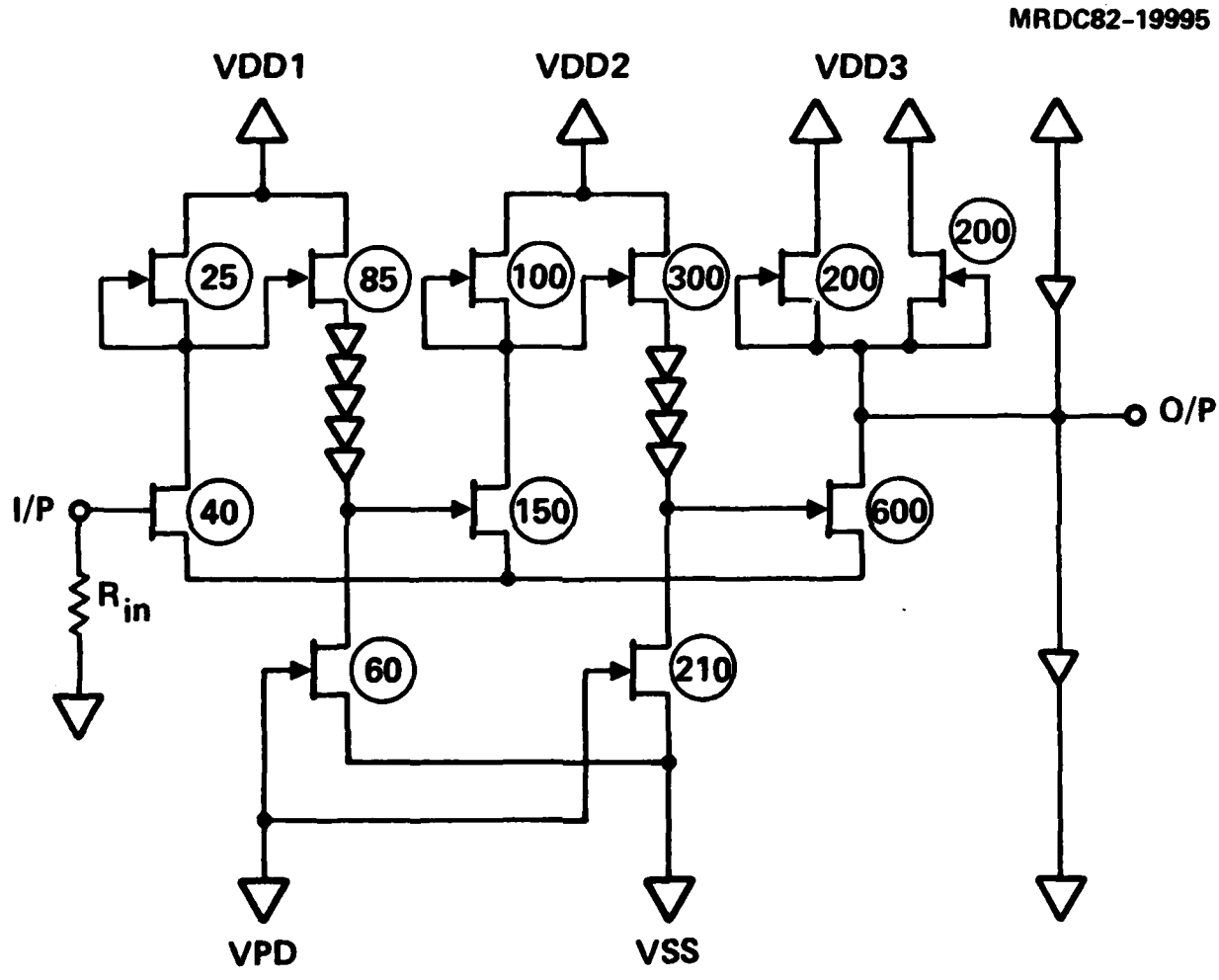

Fig. 20 Schematic of the monolithic clock-driver circuit in RA-1 chip B. Figures in the circles are the FET widths. Pinch volts for this design is two volts.

minimizes charging delays although they do dissipate more power there. The principal reasons for the use of such circuitry in these "linear" applications of clock boosting and input/output signal amplification is the excellent band-width shown by this approach and its capability of employing negative feedback to improve gain flatness, straighten out phase response and give excellent performance overall.

3.2.3 Wide Band Moderate Gain Amplifiers

The circuit shown in Figure 21 is a wideband amplifier which should provide a moderate gain of 6 db per stage or a total gain of about 12 db per amplifier from very low frequencies to 4 GHz. We have designed this amplifier using the Buffered FET approach with the addition of a small percentage of negative feedback per stage. These amplifiers are a copy of the same type of amplifiers as reported by Hornbuckle [3]. The methods of fabrication differ in small detail but the FET characteristic should be the same providing a useful broadband amplifier.

3.2.4 Clock Generator Chip

The use of OR/NAND gate dividers in the divide by 2 circuits allows the possible use up to the 1 GHz clock frequency (2.0 GHz input frequency). The Figure 18 illustrates how the complementary clock generator and two divide-by-two circuits used to provide four phases from one input signal of twice the desired clock frequency. The most desirable feature of this design is the ability to change frequency quickly without elaborate adjustment necessary to maintain the clock phases in the proper phase relationship with respect to each other.

3.2.5 High Gain, High Impedance Differential Amplifier

A circuit with a very high degree of usefulness in CCD application is the differential amplifier. In Figure 22, a GaAs FET (dual gate device) differential amplifier which has been developed in this

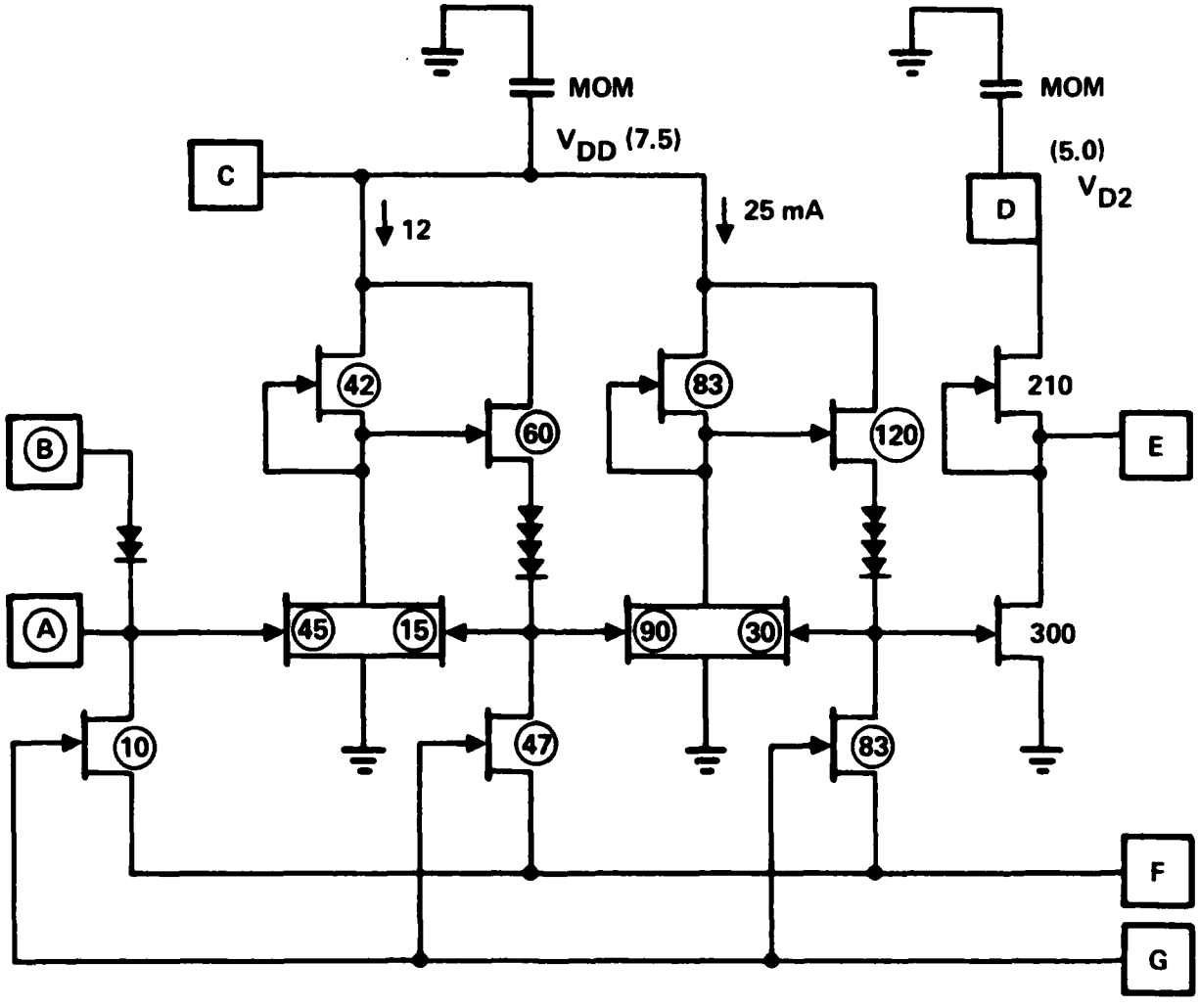

Figure 21. A broadband d.c. coupled amplifier of moderate (12 dB) gain. The figures in circles indicate FET width. The design pinch-off voltage for this circuit is 2 volts.

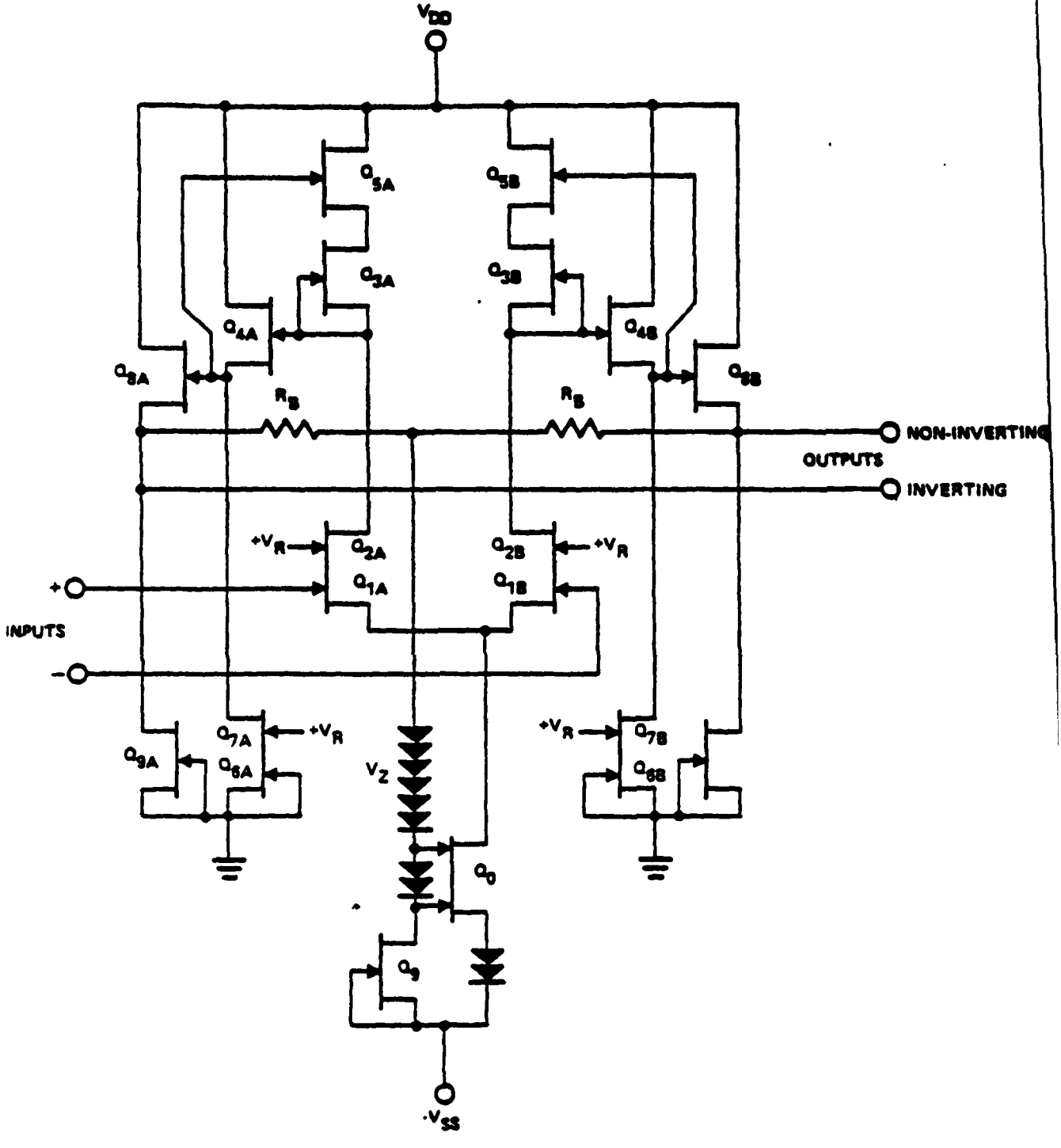

Fig. 22. High-gain GaAs MESFET differential amplifier stage using a dual-gate (CASCODE) amplifier with bootstrapped active load. This configuration achieves high gain even with relatively low drain resistance FETs. V_R is a constant bias voltage (ac ground).

laboratory is shown. We have included this device in its latest variation in the Support Circuits Program. The projected performance is 10 db of gain at up to 1 GHz. The device includes a special form of bootstrap load and feedback system to stabilize d.c. operating points.

3.3 Mask Set RA-1

All the support circuits shown in Figure 18 were designed and incorporated into the mask set RA-1.

In addition to the mentioned support circuits, a limited experiment in implanted CCDs was also incorporated in this mask set. Certain ideas of how implantation can be utilized to improve the charge transfer efficiency were to be tried out.

The organization of the RA-1 mask set is as follows: There are three basic reticles or chips, A, B and C, arranged in a 4.1 mm square as shown in Figure 23. This square ABBC is stepped and repeated in a 10 x 10 matrix so that a full size wafer is processed into 200 B chips, 100 A chips and 100 C chips. Each of these chips, which are square and 2 mm on a side, may be sawed out and each of them contains a consistent set of circuits.

Chip A, seen in the photograph of Figure 24 contains the CCD experiments, two pulse generators, one output amplifier and some diagnostic patterns to monitor the process.

Chip B, seen in the photograph of Figure 25, contains two clock driver circuits and two differential amplifier circuits. All the circuits in this reticle use FETs with pinch-off volts of over 2 V. Process diagnostics are also found on this chip.

Chip C, seen in Figure 26, contains the clock generator circuits which employ FETs with pinch-off voltages of about 1.25V. These circuits are of the SDFL type and the appropriate process monitoring for this active layer is on Chip A. Four of the wideband amplifiers using 2 V pinchoff FETs are also placed on this reticle.

To fully process all the circuits of this mask set was a 9-step process because of the necessity of adding two extra active layer implants to the basic GaAs SDFL process. These extra active layers are the CCD

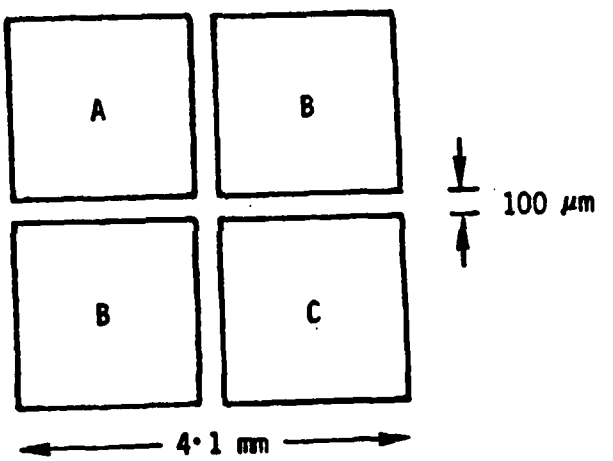

Figure 23. The composite reticle for support circuit mask set RA-1.

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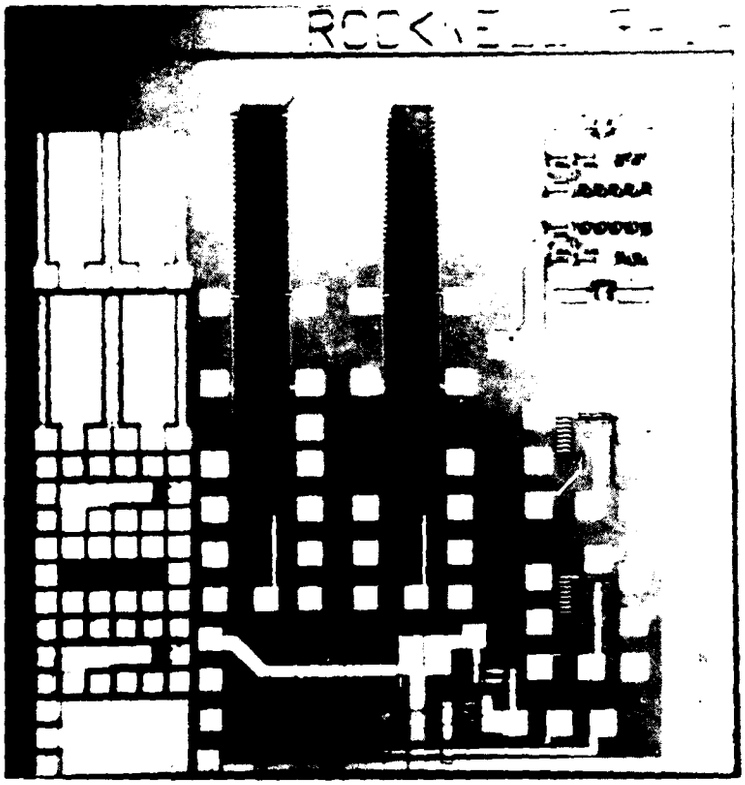

Fig. 24 Chip A which contains process monitoring, two CCDs, two pulse generators and one output amplifier.

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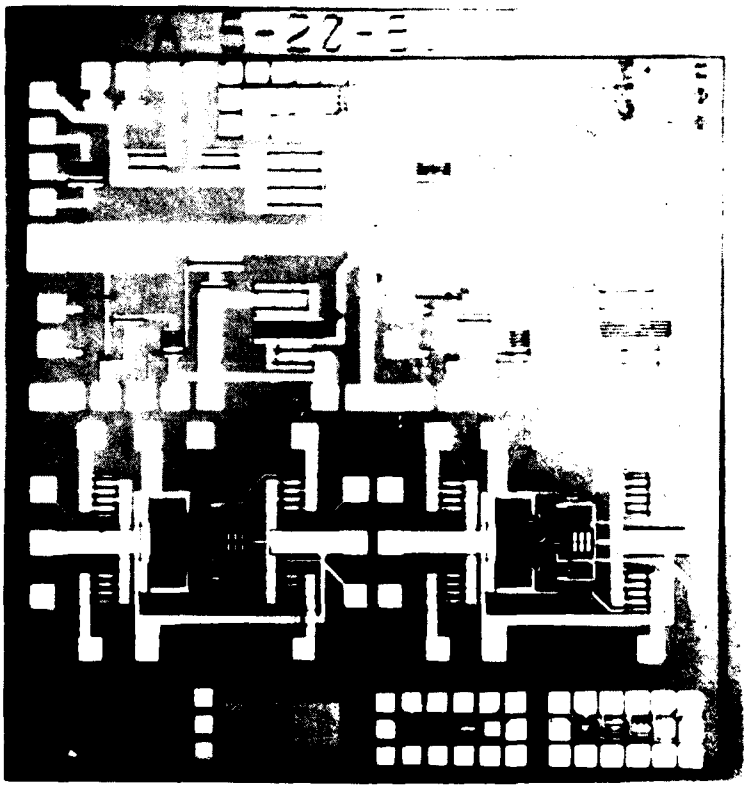

Fig. 25 Chip B which contains four clock driver circuits, alignment marks and process monitoring.

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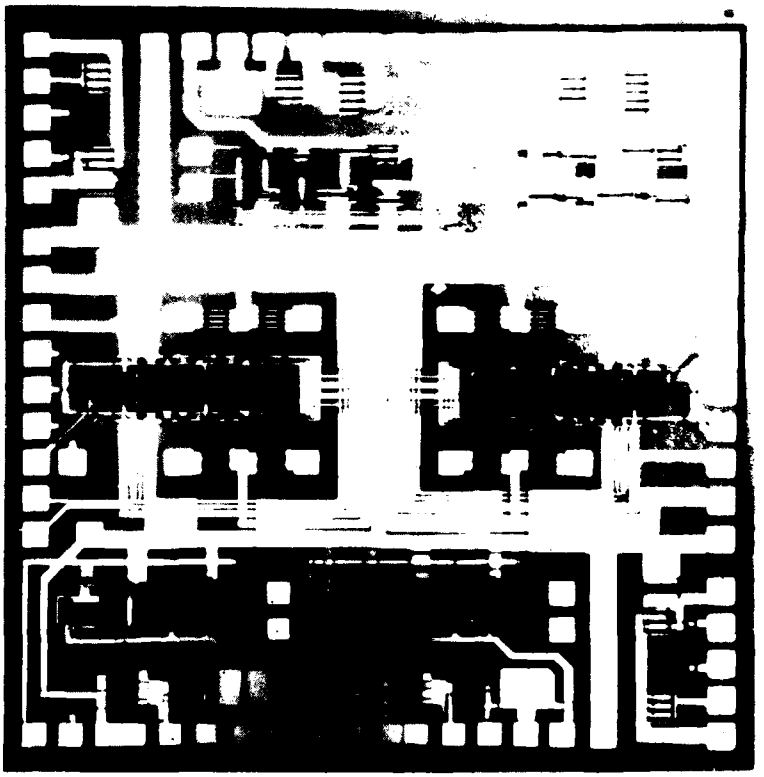

Fig. 26 Chip C which contains the clock generation system and four amplifiers.

active layer and the buffered FET circuitry which have pinch-off voltages of 3.5 and 2.0 volts respectively. In addition, it was necessary to place the CCD electrode metal (which has many 1 μm gaps) separately with a resist step in the process. In processing the first three lots of these wafers, it was decided to forego the CCD as this simplified the process considerably. In the next Section, a brief summary of the results to date from the measurements on completed wafers will be given.

3.3.1 Process Yield

Three of the five lots started using the RA-1 mask set were finished and are presently going through testing procedures. The remaining two lots shall be finished when the time and work requirements of other programs allow. The testing of these wafers began in the period around January of 1982 when the first set of wafers finished processing. Processing was suspended after three lots were completed because it was felt that these three lots would provide as much information as we would need to evaluate the circuits being produced. The testing and further processing of these devices is on a low priority because of the heavy call from other externally funded programs upon the limited manpower available. Therefore, the complete testing of the RA-1 wafers is as yet not complete and is going forward at a slow pace.

The yield of circuits on the three lots went from fair to good, i.e., with increasing experience the alignments and device quality also increased. Overall yield on the third lot of device wafers was quite satisfactory.

3.3.2 Process Evaluation

The testing of the wafer starts during processing; for example, the Ohmic characteristics and the source to drain current saturation characteristics can be tested on T1 test pattern after the Ohmic metallization during the processing. Figure 27 shows such a measurement on one of the wafers. It can be seen that the characteristics have good uniformity as

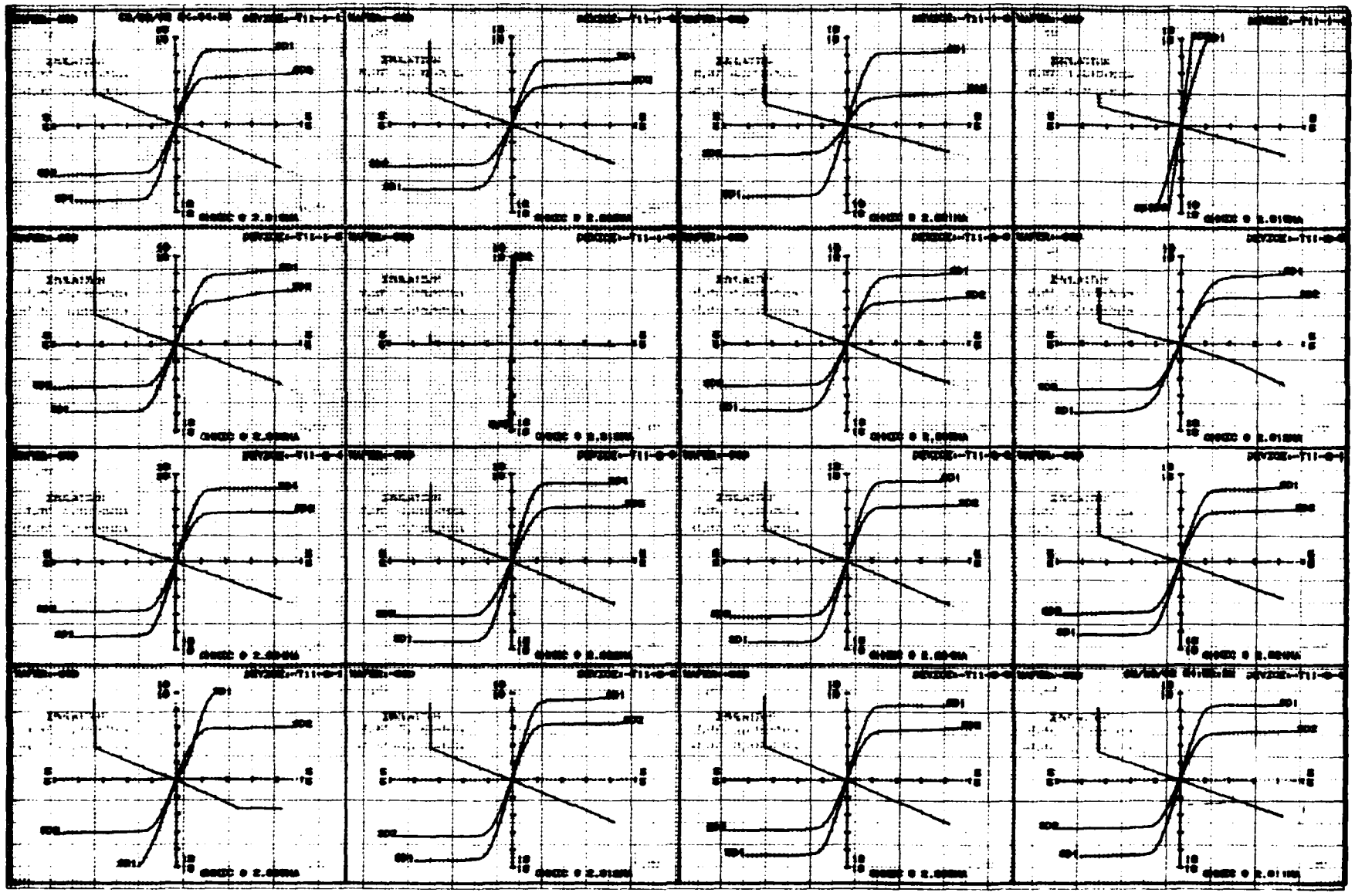

Fig. 27 D.C. Testing of the T1 test pattern on a wafer during the processing sequence. Curves labelled SD1 and SD2 are the source to drain characteristics of two gateless FETs. The straight line passing through the origin is for testing the ohmic contacts. The isolation provided by the S.I.-GaAs substrate is also tested and the numbers in the top left quadrant show the current flow between two isolated pads for ±5V applied

the measurement is repeated on successive dies on the wafer. A few of the "bad" characteristics are obviously a test pattern situated close to the wafer edge.

Figure 28 shows the measurements made on a finished wafer. The pattern tested for these measurements contain six Fat-FETs. The characteristics shown are the Source to Drain I-V characteristics with the Gate held at the source potential for the six FETs of varying Gate-lengths. At the end of each I-V plot is shown the pinch-off voltage for that FET. Here again, it can be noticed that the characteristics have good uniformity in the test regions away from the edge of the wafer.

After the test patterns are measured and evaluated,the functional testing of the various circuits is undertaken. Initially, they are tested for their d.c. characteristics and their operation at low frequency using the conventional probe-cards on the wafer. The clock driver circuit in reticle B was the first circuit measured in this manner.

3.3.3 Dc Testing of Clock-Driver Circuits

Figure 20 shows the schematic of the clock-driver circuit. This circuit accepts its input from one of the four clock phases provided by the clock generator circuits on Reticle C and is designed to provide enough power to drive a 150 ohm load. Before these circuits could be functionally tested on the wafer, DC testing was required; first to identify the chips with good device components and then to establish the proper operating conditions.

In the first test, the I-V characteristics of some important components like the 200 μm FETs which provide the output drive, the level shifting diodes stack and the two clamping diodes at the O/P are measured and plotted for each circuit. Figure 29 shows a sample of such measurements which then allows us to select good circuits for further testing.

In the second test, suitable DC biases are applied while the voltage applied to the gates of the Pull-Down FETs, V_{pD}, is varied and its effect on the operation of the circuit is studied by monitoring the current and voltage levels at various nodes in the circuit.

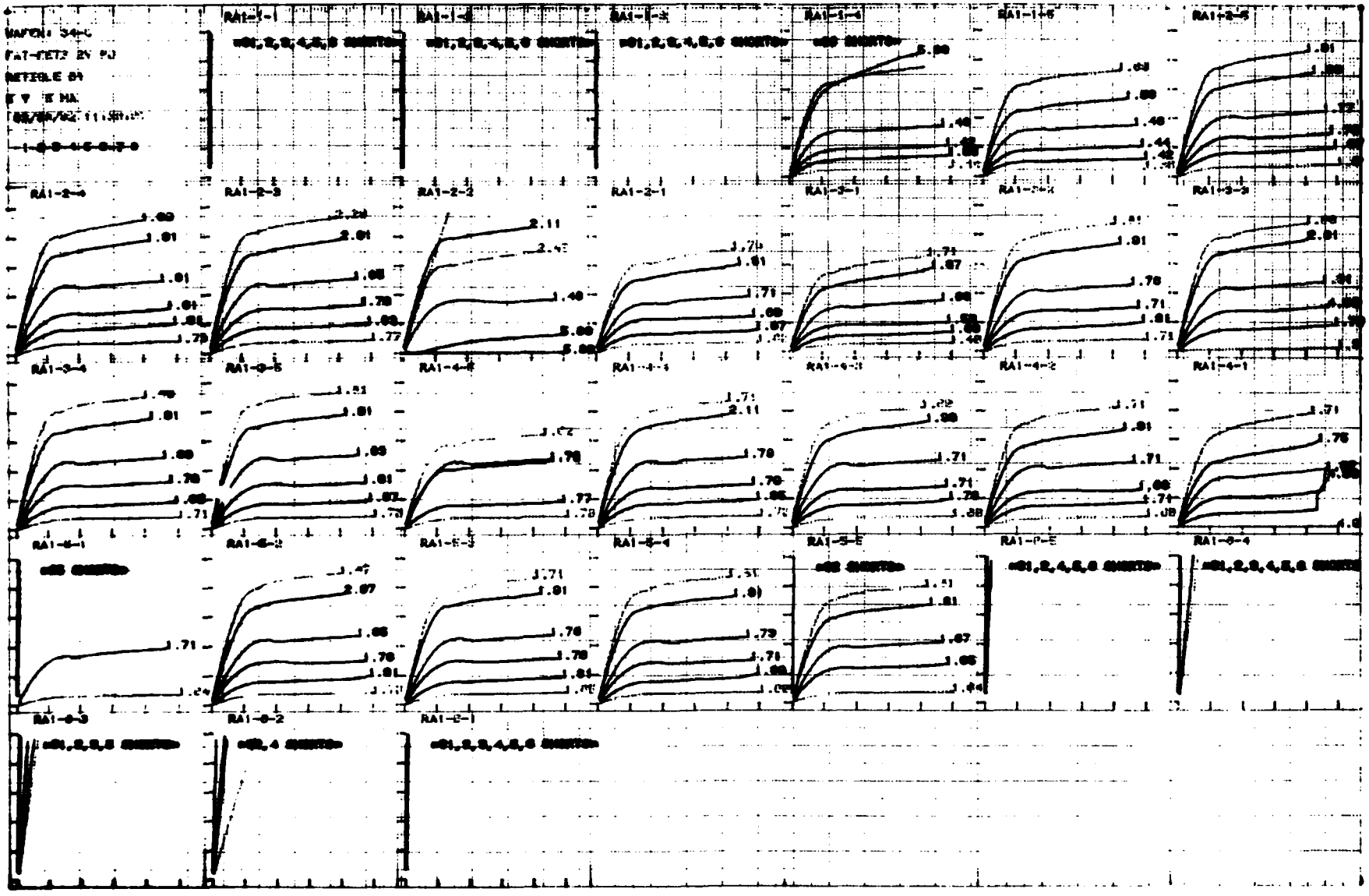

Fig.28 D.C. Testing of the Fat-FETs test pattern on a completely processed wafer. The six FETs in the test Pattern have the gate length varying from 1μm to 50μm for 50 μm wide gates. The numbers at the end of each curve shows the gate bias required to pinch-off the current in the source to drain chanrel to 2% of its zero bias value.

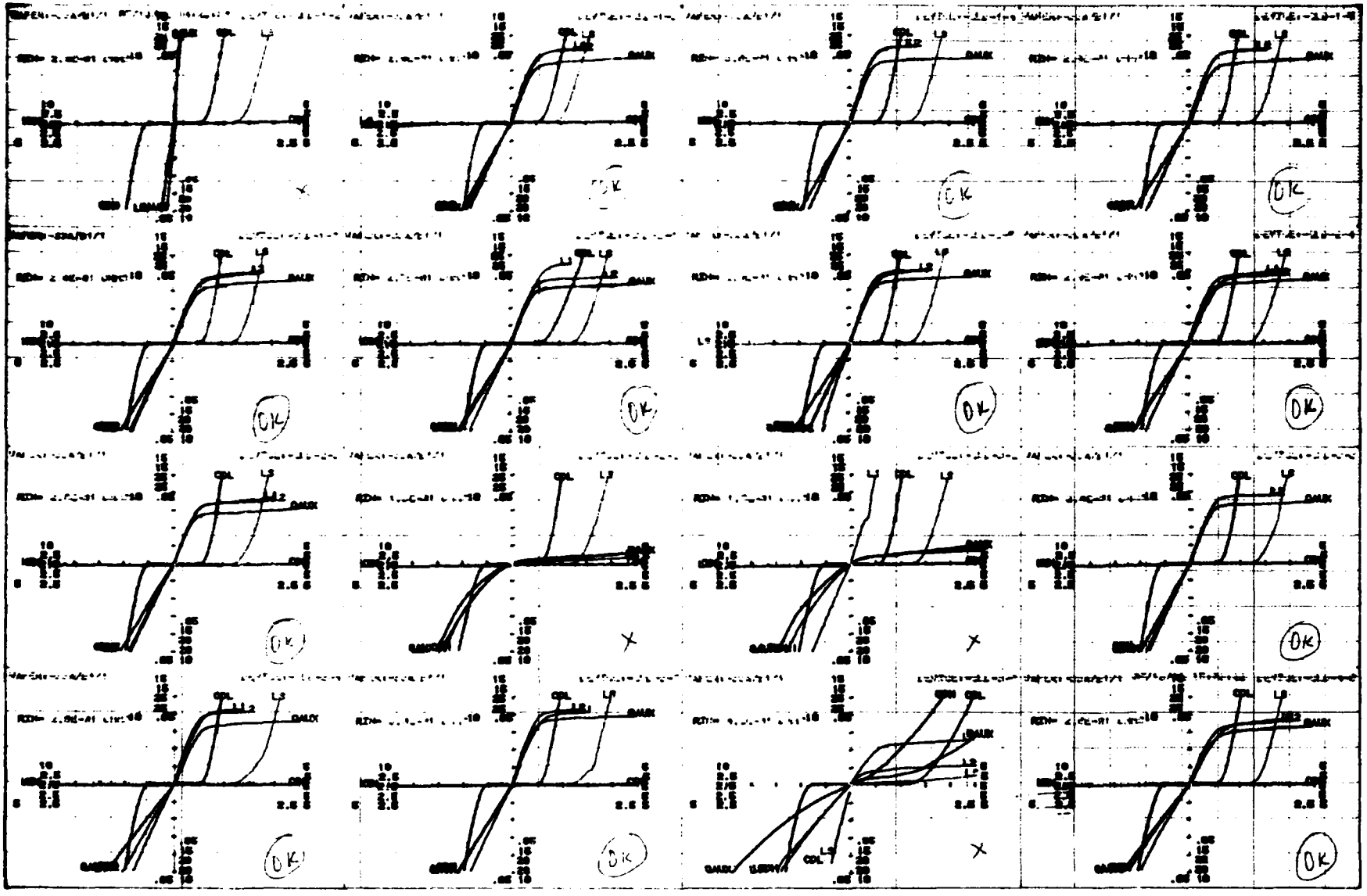

Figure 29. Results of the first D.C. testing of the Clock-Driver circuits on wafer No. 33A. The plots showing the normal characteristics for the FETs and diodes tested are marked OK and go through the second D. C. testing.

Figure 30 shows a typical plot obtained during such a measurement on a good clock-driver circuit. These plots are obtained by a partially automated test set-up on an eight-color plotter and therefore the various parameters are more easily identifiable than shown in this photocopy. Basically, what we learn from such testing is that the optimum V_{PD} value for this circuit will be about 1. Volt below the V_{SS} level.

The DC operational testing of the clock-driver circuits on the three finished wafer lots is currently underway in the manner described previously. There are up to 6 x 6 composite reticles on each wafer and four clock-driver circuits on each such reticle, i.e., there are up to 144 circuits per wafer to be tested. We are, therefore, also working towards making the test set-up completely automatic. This work involves reconfiguration of the test equipment, modifying some of the programmable power supplied and revising the software for testing sequence and data acquisition.

3.3.4 Functional Circuit Testing

To date, functional measurements have been conducted using probe systems to evaluate the devices of the three lots of RA-1 that have been finished.

The clock driver of Reticle B is perhaps the most useful circuit in the mask set providing (as it was supposed to) a high frequency square wave at the clock electrode terminals of the CCD of sufficient magnitude to provide the required clocking power. The high speed tests were conducted using a non-ideal system to apply signal and bias to the devices which were still in the wafer. In other words, we did not dice the wafers and place them into packages. This economy in manpower and expended effort is compensated by the fact that many more devices could be qualitatively evaluated this way in a short time even though the use of a probe system would not allow going to the ultimate frequency desired for testing of these devices.

The input and output waveform of a typical clock driver circuit from wafer RA-1 is shown in Figure 31. The frequency of the square wave

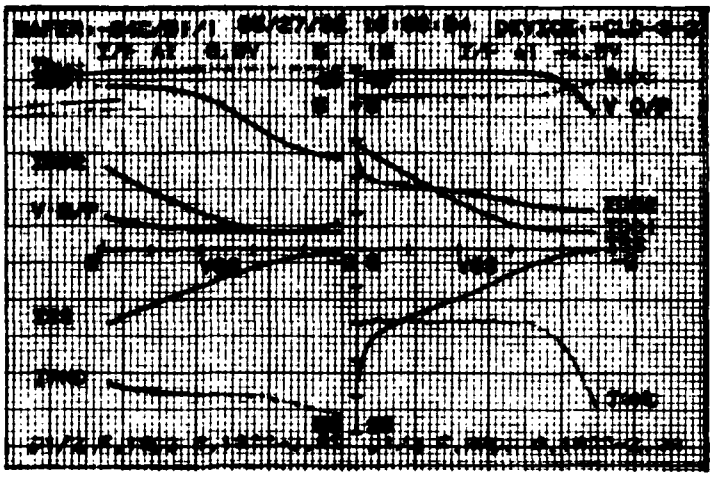

Figure 30. D.C. Testing of the clock driver circuit. IDD1, IDD2, IDD3, ISS and the IGND and plotted along with the V O/P (thick line) as a function of VGS for the pull-down transistors. The plots on the left-hand side are for an input level of 0V and the plots on the right-hand side are for the input voltage of -2V. The supply voltages for this test were: VDD1 = VDD2 = 5V, VDD3 = 7V and VSS = -3V. At VGS = -1V (i.e., VPD = -4V), this circuit will provide an output voltage swing from 0.65V to 5.1V into 150 Ω load.

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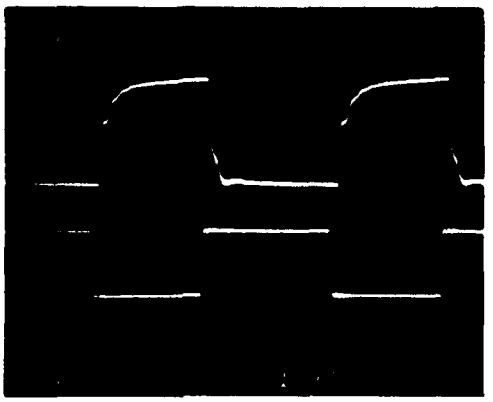

$V_{DD1/2}$: 6.31

V_{DD3}: 8.19

V_{SS}: -1.79

V_{PD}: -0.98

Fig. 31 Functional testing of the clock driver circuit of Fig. 20 at 2.5 MHz. An 8 volt V_{DD3} provides a 5V pp output signal into a 150 ohm load.

is 2.5 MHz and the operation is providing a ± 2.5 V swing for a V_{DD3} of 8.19 volts. A peak-to-peak swing of greater than 6 volts is achieved when the V_{DD3} is greater than 10 volts D.C.

In Figure 32, at a frequency of 150 MHz and moderate value of V_{DD3}, a swing peak-to-peak of 4.0 volts is achieved. It is felt that at this frequency, the limitations of the probing system are beginning to limit the response of the circuits.

The clock driver circuits of Reticle B do work and so does the clock generator circuit of Figure 18. This is the circuit in Reticle C containing the complementary clock generator and the two divide by two circuits. In Figure 33, the input and output waveforms of this circuit chip are shown operating at a low frequency. This is a very complex chip yet quite an appreciable number of these devices were found to be working after a proper adjustment of the bias levels. As stated before the testing of the circuits on the RA-1 mask set is going forward at a slow pace due to the press for more work on the CCD devices. The order of priority will be to a) perform more testing on the clock generator at higher speeds; test the wideband amplifiers at low signal levels; c) test the pulse shaping circuits and d) test the differential amplifiers. Finally, if time allows, the hybrid assembly of all these chips into an r.f. test fixture of the type depicted in Figure 7 must occur.

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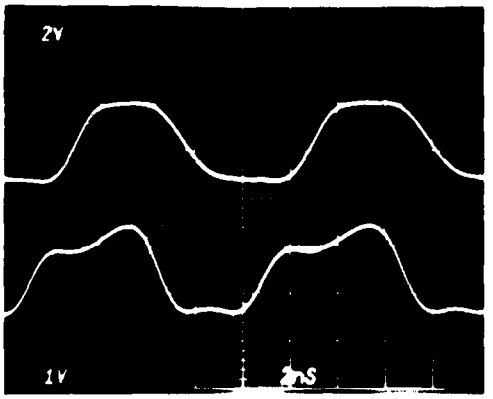

$V_{DD1/2}$: 5.04

V_{DD3}: 7.5

V_{SS}: -2.46

V_{PD}: -2.95

Fig. 32 At 150 MHz the clock driver circuit is capable of supplying 4V pp into a 150 ohm load using just 7.5 volts V_{DD3}.

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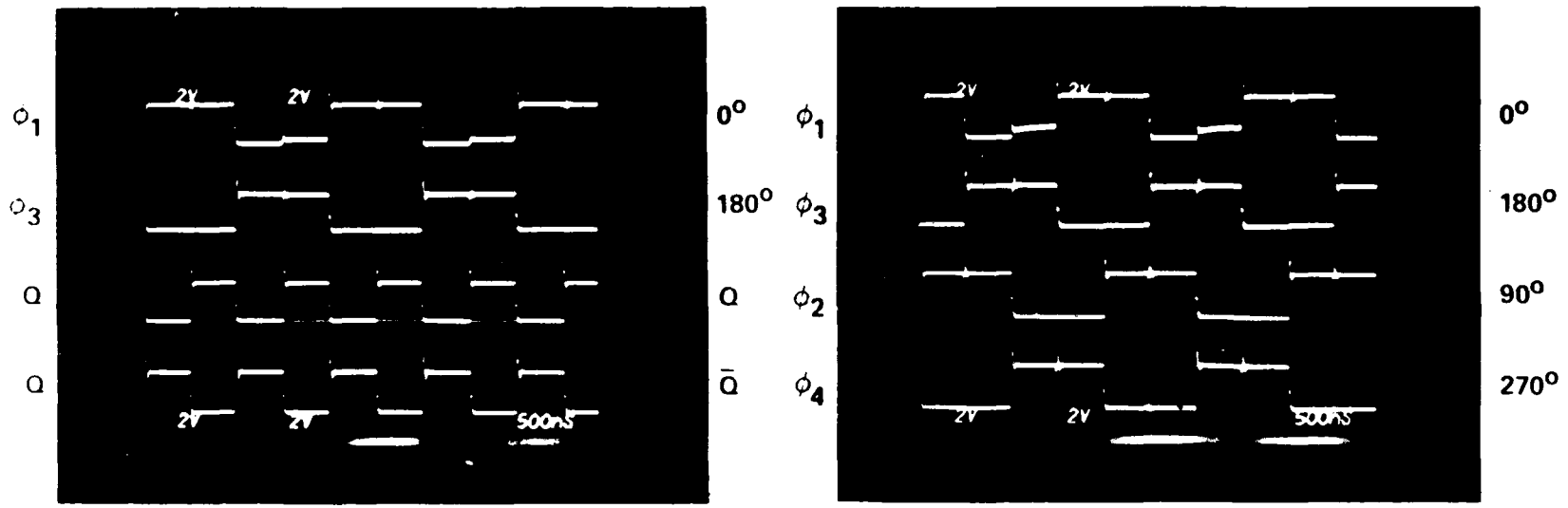

INPUTS (LOWER), OUTPUTS (UPPER)
OF ÷2 CIRCUIT

÷2 OUTPUTS

Fig. 33 The operation of the chip generator chip is seen in these photos illustrating the divide by two actions and the proper phasing of the clock driver.

4.0 SUMMARY AND CONCLUSIONS

The direct implantation of CCD layers in a manner consistent with the GaAs FET Integrated Circuit technology is not an easy accomplishment. From materials measurement it is obvious that it is difficult to obtain a consistent level of activation at the low doses required for the CCD but that the uniformity of the product layer is also not within acceptable limits. Device measurements indicate a considerable level of bulk trapping which contributes to a CTI which is too large.

Alternative methods of obtaining the deep layers necessary for CCDs only offers one more method which is easily compatible with IC planar technology. This is implantation into clean buffer layers. Device evaluation to check on this possibility is presently underway. The implantation at elevated temperatures into buffer layers did produce layers that were more uniform than those obtained in the direct implantation into melt grown substrates and preliminary indication are that the activation might be higher. However, the most telling test will be the device behavior which will betray the presence of traps if they are there.

If hot implantation into epitaxially grown wafers proves to be unsatisfactory then the only methods to obtain the CCD layer are to use epitaxial growth. This means usually an uncompatibility with a planar process.

The design of support circuitry for CCDs was accomplished. The list of circuits designed for initial evaluation is as follows:

1) clock generators
2) clock drivers
3) pulse shaping circuits
4) wideband amplifiers (4 GHz)
5) Differential amplifiers

These designs were incorporated in a mask set called RA-1. Five wafer lots were started and three of these brought to completion. The remaining two lots await completion at another date.

Devices tested to date are the clock generators and the clock drivers. The clock generator and clock driver circuits performed quite within their expected limits and the performances indicated that with the proper conditions applied, they will perform usefully up to very high frequencies (500 MHz).

Further testing will be conducted as time and funding allow.

REFERENCE LIST

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